Focused Ion Beam (FIB) Circuit Edit

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Introduction

While focused ion beam (FIB) circuit edit has been used for quite some time on older process nodes, it now offers even more important benefits as the industry migrates to smaller technologies. The stakes are rising at 28 nm and beyond, and it can now cost $10 million or more to bring a device to market. Manufacturers looking to mitigate risk are using FIB circuit edit to reduce costs while also improving design performance and functionality, cutting design time for complex devices.

Many of the problems encountered at advanced process nodes cannot be predicted from the experience gained during previous design projects. Part of the solution to advanced design challenges is now coming from electronic design automation tool providers, who offer design-flow advice and other recommendations.[1] Historically, FIB circuit edit enables developers to significantly improve the process of debugging and validating fixes or exploring design optimization changes before committing to a full mask spin and its associated costs and time requirements. In addition to applying new design-flow modifications, developers can also apply FIB circuit editing with their early prototypes during debug. The same techniques can be used to explore design optimization opportunities by quickly and inexpensively implementing and creating physical prototypes, again eliminating the need for a trial-and-error approach with repeated mask versions.

What about devices manufactured using widely adopted legacy processes? Designers are exploring new circuit functions, updating topologies, and increasing analog content, voltages, and frequencies far beyond what was originally attempted at these legacy nodes. As designs become more complex at older nodes, there is greater risk that well-understood failure mechanisms, such as electrostatic discharge and latchup, may not be reliably prevented by traditional design practices, even though these practices worked well for less-complex designs. For these reasons, FIB circuit edit continues to be as important at these older nodes as it has always been, with continuing benefits in terms of a reduction in mask spins and faster time to market.

How FIB Circuit Edit Works

While FIB systems are used in a number of applications throughout multiple industries, their primary use for semiconductors is circuit modification, that is, cutting traces and depositing localized metal connections or insulators (Fig. 1). Using today's latest equipment, it is possible to edit circuits fabricated with 28 nm and smaller technology nodes that feature multiple-layer metal stacks and occupy flip chip and other advanced chip-scale form factors.

A finely focused gallium ion beam with nanoscale resolution is used to perform FIB circuit edit and enable operators to image, etch, and deposit materials on an IC with an extremely high level of precision.
Circuitry is cut and connected within a functional device by removing and depositing materials. This process is also used to create probe points for electrical test. The high-energy gallium beam can mill through conductors; it uses various gas-based chemistries to either enhance milling precision or more effectively deposit conductive and dielectric materials. For instance, by selecting appropriate gases, a choice of tungsten, platinum, or silicon dioxide can be very precisely deposited using the ion beam.

The FIB tool is coupled to a computer-aided design (CAD) navigation system, making it possible to locate the area of interest. The designer’s graphic display system (GDS) files are typically used to navigate to a precise area. This provides a method to find subsurface features and ensure that the correct edits are made (Fig. 2). Accurate beam positioning is one of the most critical requirements for FIB circuit edit.

Multiple Uses for FIB Circuit Edit

There are a wide variety of FIB applications. Typical applications include:

- **Production device debugging and optimization**: FIB circuit edits are often performed after a design flaw has been identified in production devices to ensure that the proposed modification will completely resolve the problem with, at most, one mask spin. This speeds the process of delivering working prototypes to customers so they can continue software development, which is increasingly important in mobile device and other market segments with short cycle times.

- **Duplicating and scaling fixes**: After FIB circuit edit has been used to verify a fix on a prototype, it is then possible to duplicate that fix on other devices that can be provided to internal test, validation, and qualification teams and even as samples to the customer. This enables further system or application development work to continue in parallel as the organization waits for a new mask spin and final production devices to be delivered.

Figure 3 shows the best approach for integrating FIB circuit edit into the overall IC development and testing process.

Ongoing FIB Circuit Edit Improvements Eliminate Complete Reliance on PDFD

In the past, it was assumed that FIB circuit edit, especially at advanced nodes, could not be implemented without physical design for debug (PDFD). The assumption was that effective FIB circuit edit required the use of preplaced PDFD features for navigation, logic, and timing modifications as well as signal probing. Typical recommended features include bonus combinational and sequential cells, fiducial markers, mechanical probe access points, FIB access points (such as those designed into clock buffers and other standard cells), and building-block cut-and-connect cells that enable spare circuits and features.\[^2\]

In reality, however, FIB circuit edit has advanced to the point where it can be performed without PDFD, although PDFD features do enhance debug and FIB circuit edit success rates. One of the reasons the industry had assumed the need for PDFD was the belief that scaling, layout efficiency, and new technologies such as trigate reduced the capability of FIB circuit edit to access transistors and metal signals. The PDFD proponents point to the fact that moving to advanced nodes has dramatically reduced “open” space, thereby creating insurmountable challenges related to mill selectivity, resolution, end pointing, and invasiveness and thus creating the need for PDFD features that would provide guaranteed access to critical signals. These issues are mitigated, due to the latest advances in FIB circuit edit tools and techniques, and make costly PDFD features—while certainly helpful—no longer mandatory. As an example, a multilegged clock inverter at small geometries can be trimmed...
successfully using today’s advanced FIB circuit edit capabilities without damaging the unrelated adjacent device and without requiring prior insertion of increased spacing between adjacent transistors by PDFD feature placement in clock elements.[3]

One of the most important developments has been in the capability of FIB circuit edit tools to provide better aspect ratio for smaller cuts. Today’s systems also deliver advances in areas including ion beam resolution, operating software, and CAD navigation. Ion beam resolution advances alone have delivered significant new capabilities that are critical for recognizing small features, aiding in visual endpointing, enabling precise CAD alignment, and improving box placement accuracy.

Tool advances are only part of the story. Because FIB tools are not entirely automated, there is no underestimating the critical importance of FIB operator experience to circuit edit success. For example, endpoint detection (the ability to know when selected layers of interest have been successfully etched) continues to require a high level of skill to achieve success.

**Optimizing FIB Circuit Edit Success**

There are numerous prerequisites for FIB circuit edit success, including:

- **Tools:** High resolution is particularly important at advanced nodes such as 28 and 20 nm. To make these edits, designs generally require a 0.1 μm resolution as well as a trenching approach that supports a finer resolution. The smallest hole that can be made with today’s equipment is 0.1 × 0.1 μm with an aspect ratio of 1/20. For most 20 and 28 nm designs, it is impossible to make a small-enough hole to reach the target. As a result, specialized FIB techniques are required in order to use lower aspect ratios and gain access to the target. The system must be able to smoothly remove dummy metal above the target metal layer. This also requires deep and extensive knowledge of IC circuitry and processes, FIB tools, and ion milling patterns. Figure 4 shows a typical backside trench.

- **Backside editing:** Backside editing is frequently the most effective way to operate on flip-chip packaging. This may be true because of the substrate material in flip-chip packaging or because of the increased number of metal circuit layers in today’s ICs, which make it more difficult to reach a lower layer when editing from the top. Figure 5 shows a backside FIB circuit edit in which a resistor is introduced across two nodes.

In another example, Fig. 6 shows a backside FIB circuit edit in which a probe pad is formed for microprobing. In a typical backside edit example, the GDS file is first evaluated to identify conflicts between design and edit. The next step is sample preparation, in which the back of the package is thinned to approximately 100 μm. These parts are then tested for electrical functionality, because sample thinning may stress or damage them. Next, four-corner trenching exposes reliable reference points for aligning and locking devices and layout for precise navigation. Then, a delicate milling process is required to create a fifth, 150 × 150 μm trench over the edit area. Specialized skills and a high level of accuracy are needed to ter-

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**Fig. 4** Today’s trenching approaches support fine-enough resolutions to enable FIB circuit edits at advanced nodes.

**Fig. 5** Backside FIB circuit edit is used to introduce a resistor across two nodes.
terminate the bottom of the trench at approximately 2 to 4 μm from the active area. Finally, a series of proprietary techniques are used to perform the actual backside FIB edit. Even at these microscopic thinning, milling, and editing dimensions, today’s FIB edit techniques yield high success rates when performed correctly.

- **Handling copper layers**: Most 28 and 20 nm devices are copper devices that feature a crystal structure which is very difficult to remove smoothly. Special methods are required, as well as an experienced operator, to remove the metal smoothly with a very high level of quality. Accurate beam positioning is more challenging for copper metal devices due to the nonvisibility of the circuit patterns. This is also important for aluminum metal devices if there are no unique patterns to recognize on the top level. These issues are more challenging the greater the number of layers involved.

- **Companion failure analysis and test tools, expertise, and capabilities**: Because most devices must ultimately find their way into packages, there should be a smooth transition to decapping or delidding the devices and performing microprobing and other debugging tests on FIB-edited parts.

- **Front-end expertise**: In addition to presenting challenges due to ever-shrinking nanoscale geometrics, semiconductor advanced technology nodes also introduce new front-end materials as processes evolve. The FIB circuit edit labs can benefit from being part of a larger lab environment characterized by a significant level of front-end process understanding and materials expertise. Labs that support process research and development activity and yield support will be able to offer an advantage and insights as well as other knowledge that will help maximize the success of FIB circuit edit strategies.

### Value Increases as Risks Grow

Integrated circuit design verification and validation will continue to increase in difficulty as the industry moves down the nanoscale geometry curve, making FIB circuit edit an increasingly valuable tool for improving design success. Due to advances in both tool technology and best practices, FIB circuit edit can be used at advanced nodes for a variety of purposes, including debugging and validating fixes as well as earlier in the process to explore opportunities for design optimization without committing to a full mask spin.

### References


### About the Author

**Taqi Mohiuddin** joined Evans Analytical Group in 2013 to lead sales and marketing for the Microelectronics Test and Engineering Division. He has over 18 years of diverse experience with startup, early growth, and established multinational corporations in software, systems, and semiconductor market segments. Mr. Mohiuddin’s previous roles include leading solutions marketing for Motorola Solutions Enterprise Networks Division, vice president of marketing and business development for Siverge, and executive director of marketing for Mindspeed Technologies. Mr. Mohiuddin holds an MBA from DePaul University and a B.S. in electrical engineering from the University of Illinois at Chicago. Mr. Mohiuddin is also the co-author of a LabVIEW programming book.