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WHITE PAPER

Low Parasitic HBM Testing

The Human Body Model (HBM) Electrostatic Discharge (ESD) test is the oldest and most widely used ESD test in the electronics industry. The JEDEC HBM test isn't static; it has been revised to keep up with the rapid changes in the semiconductor industry. The latest revision of the spec addresses failures that are caused by parasitic impedances in HBM testers. EAG has the equipment and expertise to help you solve your HBM test problems.

EVOLUTION OF THE HBM SPEC

The current ANSI/ESDA/JEDEC HBM test, JS-001-2014, evolved from the military ESD testing spec, MIL-STD-883, Method 3017.8. The first JEDEC version of the spec was published in 1995. Over the last twenty years, incremental improvements have been made to the HBM spec based on the data and analysis performed by reliability engineers from a cross-section of the IC industry. One of the main goals has been the reduction of the cost and time required for HBM testing. Other changes have addressed issues with the HBM simulator hardware. The following table summarizes the different revisions of the HBM spec:

Spec	Published	Changes
JESD22-A114	1995	Almost identical to MIL-STD-883, Method 3015.8
JESD22-A114-A	October 1997	Minor changes to MIL-STD-883
JESD22-A114-B	June 2000	1 pulse/pin/polarity, 0.3 seconds minimum between pulses
JESD22-A114-C	January 2005	0.1 seconds between pulses; stress both non-supply and no connect pins, detection of the trailing EOS pulse
JESD22-A114-C.01	March 2005	Minor editorial corrections only (deleted unused figure 3)
JESD22-A114-D	March 2006	No connect pins to be left floating at all times
JESD22-A114-E	January 2007	Elimination of pre-pulse voltage rise; use of 10K ohm shunt resistor
JESD22-A114-F	December 2008	Addition of alternate (reverse) pin combinations
JS-001-2010	April 2010	First joint ESDA/JEDEC spec; rewrites of sections on apparatus and equipment qualification
JS-001-2011	March 2011	Reduced non-supply stressing (Table 2A), IO-IO stressing for differential pairs, single polarity supply-supply testing, first allowance of 2 point HBM tester for die only shorted supply pins
JS-001-2012	January 2012	New section added to describe low-parasitic HBM simulators and how they may be used
JS-001-2014	August 2014	Addition of section on testing a statistical sample of cloned non-supply pins; minor changes to definitions and Ips values

IDEALIZED MODEL OF THE HBM TESTER

An idealized model of an HBM tester is shown in Figure 1.

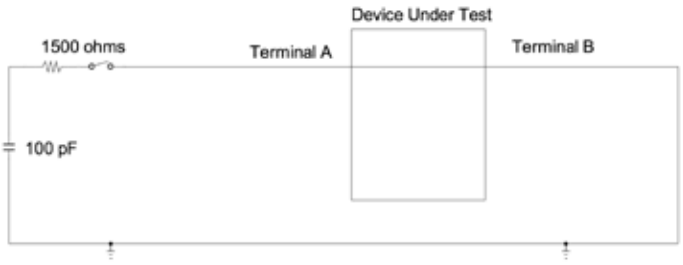

Figure 1: Idealized HBM Tester

In this model, a 100pF capacitor is charged with a high voltage power supply, not shown in the diagram. The supply is removed from the circuit, and the capacitor is discharged through a 1500Ω resistor. In this case, the device under test is the simplest one possible: a piece of wire. If you measure the current through the piece of wire as a function of time, the waveform looks like the one shown in Figure 2.

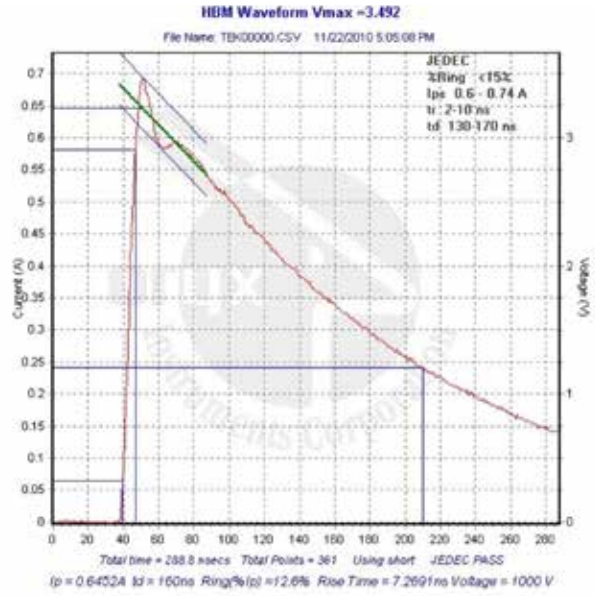

Figure 2: HBM Current vs. Time, +1000V HBM

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A MORE REALISTIC MODEL OF THE HBM TESTER

The waveform in Figure 2 shows some ringing, suggesting that there are parasitic impedances in the circuit. Parasitic impedances are any combination of extra unwanted passive devices (resistors, capacitors and inductors) in the signal path. For the discharge of an HBM simulator through a piece of wire, a more realistic circuit is shown in Figure 3.

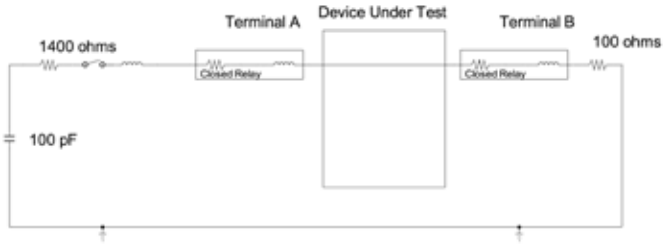

Figure 3: A More Realistic HBM Tester Model

Because relays are used to connect the terminals of the device under test (DUT) to the HBM tester, parasitic inductance and resistance is added to the discharge path. In real HBM simulators, the 1500Ω resistor is distributed, with approximately 1400Ω on the Terminal A side and 100Ω on the Terminal B side. The resistance is divided in order to provide an in-spec waveform across the entire relay array.

Because most IC devices have more than two terminals, the situation is more complicated. Every pin on the device has a capacitively-coupled impedance path to the HBM simulator, whether the pin is connected or not. When one pin of a multi-pin power or ground group is stressed, the other pins in that group are floated, and they add additional capacitance, on the order of 4-8pF per pin. This extra capacitance can significantly change the shape of the waveform. In addition, the DUT board and socket also add additional resistance, inductance, and capacitance, causing additional changes to the HBM waveform. Any circuitry that is sensitive to the waveform slope or to the Terminal B resistance can be affected by parasitic impedances. It is even possible to damage non-stressed pins during HBM testing because of capacitive coupling. All of these can impact the waveform and cause false HBM failures (See Reference 6.) An even more realistic model of the HBM tester is shown in Figure 4.

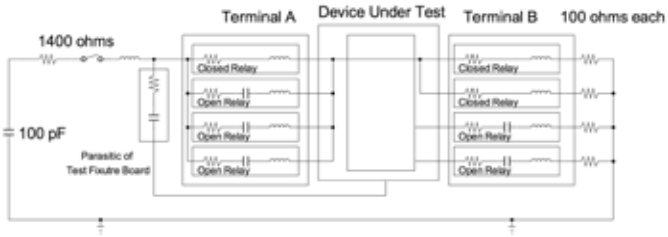

Figure 4: An Even More Realistic HBM Tester Model

A REDUCED PARASITIC HBM TESTER

To address the problems that have been seen with relay-based systems, the last three versions of the ESDA/JEDEC HBM test allow the use of a low parasitic HBM tester. The interface between the tester and the DUT is a probe station; the part is electrically connected at two points only. No special fixtures or sockets are required, and there is no relay array resulting in reduced parasitic impedance. The DUT can be a packaged part or a wafer. Critical structures can be characterized earlier in the design cycle. (See Figure 5.)

Figure 5: HBM Two Point Tester and Probe Station

The low parasitic tester provides a highly accurate and nearly perfect HBM pulse. Voltage vs time and Current vs. Time can be measured while the pulse is being applied to the DUT. This allows a more thorough analysis of the DUT's behavior during the HBM stress. (See Figure 6.)

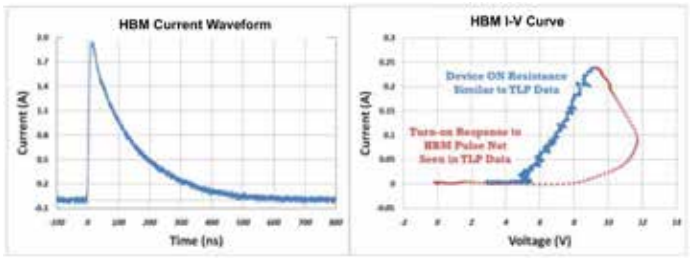

Figure 6: Two Point HBM Tester Waveform and I-V Curve

EAG'S TWO POINT TESTER APPROACH

Because a two point tester is still too slow to do tests on large production parts, EAG has adopted a hybrid test strategy, using the available relay testers.

1. Test the DUT on a relay tester. This is allowed by the spec, and it's the highest speed and lowest cost solution.
2. Minimize tester parasitic impedances by using the following practices:
   a) When a multi-pin supply or ground plane is Terminal B (grounded terminal), tie all of the pins to ground
   b) When a multi-pin supply, ground, or non-supply group is Terminal A (zapped terminal), don't zap all pins; zap a representative pin instead.

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   c) In the supply/ground to supply/ground tests, zap positive polarity only.

3. If there are no failures at ATE, the DUT has passed the test.
4. If failures are observed or if characterization data is required:
   a) Do further stressing to identify and isolate the failing pin pairs.
   b) If a pin pair passes on the two-point tester, the device passes
   c) If a pin pair fails, use the two-point tester to characterize the failure.

CONCLUSION

With the rapid changes in process technology, false failures due to relay tester parasitic impedances has become a more important HBM issue. EAG's testing approach minimizes the incidence of false failures.

EAG has the capability to determine if you have a false failure using a two-point tester. This leads to fewer mask changes and faster time to market for EAG customers. You can count on EAG to provide you with the latest standards and best testing practices available in the industry.