eurofins | EAG Laboratories

ESD & Latch-Up Testing

Our highly experienced team utilizes the most up-to-date testing methodologies for the most accurate results

Eurofins | EAG Laboratories is an industry leader in ESD (Electrostatic Discharge) and Latch up testing. Our highly experienced engineering team includes recognized experts with experience in the latest semiconductor technologies, circuit design, and device physics to optimize your ESD and latch-up testing. We utilize the most up-to-date testing methodologies that are consistent and reproducible, and deliver technical interpretation of the test data and accurate assessment of the results.

We have in-house PCB design to create custom ESD fixtures quickly to help speed your time to results. In addition, to ESD and Latch-up testing, we provide ready access to world class failure analysis, environmental / reliability testing, FIB circuit edit, electron microscopy and ATE test services.

Our ESD and Latch-up test offerings include:

- Human Body Model (HBM) and Machine Model (MM)
- Charged Device Model (CDM)
- Latch-up
- Transmission Line Pulse (TLP)

Why Eurofins | EAG Laboratories?

Eurofins | EAG Laboratories provides the specialized support and services you need to accelerate time to market, fill equipment and expertise gaps, and manage risk associated with product development.

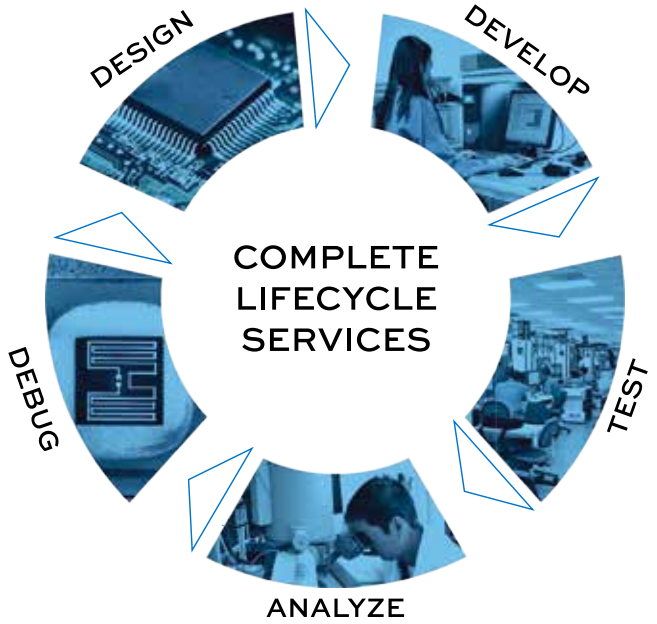
- Expertise in ESD and Latch-up with advanced product technologies
- Comprehensive HBM, MM, CDM, Latch-up and TLP testing
- Interpretation of data and detailed assessment of results
- Customized services to meet your specific needs
- Comprehensive failure analysis capability to identify root cause quickly

ESD Testing

Our ESD testing services consist of HBM, MM and CDM. Both HBM and MM range from basic Level 1 testing to Level 4 comprehensive testing with detailed engineering diagnostics. Detailed reports are delivered upon completion of testing for all levels of service. We also offer customer defined experiments that are customized to meet specific product needs. JEDEC, MIL-STD, and AEC, and ESD Association standards are strictly adhered to.
CDM testing consists of Level 1 and Level 2 testing as well as customer defined experiments that are fully customizable. We follow applicable JEDEC, AEC, and ESD Association standards.

Latch-up Testing

Although latch-up testing is performed on the same automated testers as ESD testing, the tests are dramatically different. ESD testing is an un-powered test, whereby pins receive voltage pulses with complex combinations of grounded pins on the device under test (DUT). Latch-up testing is performed with the DUT powered, and signals applied to the part to place it in a stable, low current configuration. Specialized automated testers, such as the Thermo Scientific Mk2 or Mk4, are used for ESD and Latch-up testing because each tester channel has the unique ability to be programmed as a power supply, signal pin, or stress pulse generator.
The goal in IC latch-up testing is to trigger



and monitor a latch-up event, where the stress pulse activates a parasitic “Silicon Controlled Rectifier” (SCR) structure within a CMOS or Bi-CMOS process technology. Latch-up testing is fundamentally about the chip physical layout, how circuit blocks are situated relative to one another, and how unanticipated charge is removed from physical elements in the semiconductor material.

Latch-up testing is done according to the last revisions of the JEDEC latch-up specification, JESD78B, JESD78C, or JESD78D. Testing can be done at a customer specified ambient temperature, from 25°C to 150°C.

Applicable LU Specs

- JESD78 (JEDEC)
- AEC-Q100-004 (Automotive Electronics Council)

Transmission Line Pulse (TLP) Testing

Transmission Line Pulse testing, or TLP testing, is a method for semiconductor characterization of Electrostatic Discharge (ESD) protection structures.

Transmission Line Pulse testing is useful in two very important ways. First, TLP may be used to characterize Input/Output (I/O) pad cells on test chips for new process technologies and Intellectual Property (IP). TLP is very useful in developing simulation parameters, and for making qualitative comparisons of the relative merit of different ESD protection schemes for innovative pad cell designs. Secondly, TLP may be used as an electrical failure analysis tool, often in combination with conventional, standards-based component ESD testing.

TLP testing is done according to the ESDA TLP test method, ESDA SP5.5-2003. TLP is quoted on a case by case basis, based on the scope of the work requested; estimated engineering time to perform the test, and customer requested reporting.

Applicable TLP Specs

- ESDA SP5.5-2003 (ESD Association)

Engineering Sciences

- ATE Test Development and Pilot / Production Test
- Burn-in and Reliability Qualification
- ESD and Latch-up Testing
- Debug and FIB Circuit Edit
- Failure Analysis
- Advanced Microscopy (SEM, TEM, FIB/SEM)
- PCB Design and Hardware

Eurofins | EAG Laboratories delivers comprehensive design, development, test, analysis and debug services that are differentiated by expert engineering capability and comprehensive capital equipment and processes.