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WHITE PAPER

Circuit Edit Focused Ion Beam (CE-FIB) Becomes Increasingly Valuable in High-Stakes World of Advanced Node Design

Integrated circuit (IC) designers continuing to lean on the CE FIB technique without compromising performance. The technique used on older process nodes is proving even more valuable at 20 nm and smaller nodes. Finally, the benefits of CE FIB to correct layout issues and test design changes before making such changes has increased as doing a respin during development of devices at advanced nodes takes $10 million or more to bring such a device to market.

Similar challenges face designers of power control ICs that need to reduce costs, optimize performance, and combine control with power FET functionality. In these designs the functionality, mitigation of risk, and speeding time to market for designs, will require FIB circuit edit techniques at increased rates.

It is widely understood that IC designers will encounter many new issues as many power devices move to silicon carbide (SiC). The new issues at advanced process nodes will be difficult in SiC and even more so in gallium nitride (GaN) and other wide bandgap materials.

These issues are not impossible to anticipate based on previous design work. Many EDA tool providers are already addressing these issues with tool providers. They are already addressing the difficulty of advanced materials and nodes through design flow and other methods. This isn't sufficient, however and application of FIB circuit editing with early prototypes during de-bug will be required. Applying FIB circuit editing to the process of debugging and validating fixes can also be used to explore design optimization and design optimization changes, before committing to the high cost and lengthy timetables of a full mask spin, by quickly and inexpensively implementing the proposed changes and creating physical prototypes that can be tested and validated.

TACKLING CHALLENGES AT ADVANCED PROCESS NODES

FIB-edited device prototypes can be used to guide one-time modifications to masks, eliminating the need for a trial and error process. Design success barriers are magnified at advanced process nodes, and the trial and error approach with successive versions of masks is time/cost prohibitive. At advanced nodes the mask costs are high, and it is much more difficult to find and fix bugs.

OVERVIEW OF FIB CIRCUIT EDIT CAPABILITIES

It is widely understood that designers will encounter many new problems at advanced process nodes. The CE FIB systems have several uses in the semiconductor industry, difficult if not impossible, to anticipate based on previous design nodes. Pre-silicon testing is used to check layouts of metal connections within a chip (see Fig. 1). Simulation times are growing excessive, and many designs simply cannot be 100 percent verified without physical samples. Simulation models may be imperfect for complex designs and packaging can cause stresses to sensitive devices. The need to verify the final product and make changes to improve/fix designs will remain in play.

Challenges in this environment range from multiple patterning and layout dependent effects (LDE) to the use of local interconnect layers. Design and integration complexity give rise to a new level of difficulty with each new technology node. Fast signals and high power electromigration also create challenges. Decreasing metal pitch leads to coupling effects and signal integrity issues. Increasing wire and via resistance requires more advanced and variable wire sizing and tapering techniques. Additionally, extraction, timing, signal integrity analysis, and modeling pose a multitude of issues that designers must solve before they can achieve the required accuracy on a new device. This often requires a check on a physical sample and the CE FIB allows alteration of the sample to check results from changes in the layout. The CE FIB is performed quickly and easily, at a small fraction of the $5 million to $10 million in costs that are typical for a new lot of wafers in a fab.

Using today's state-of-the-art equipment, it is possible to edit circuits fabricated with 28 nm and smaller technology nodes that feature multiple-layer metal stacks and occupy flip chip and other advanced chip scale form factors.

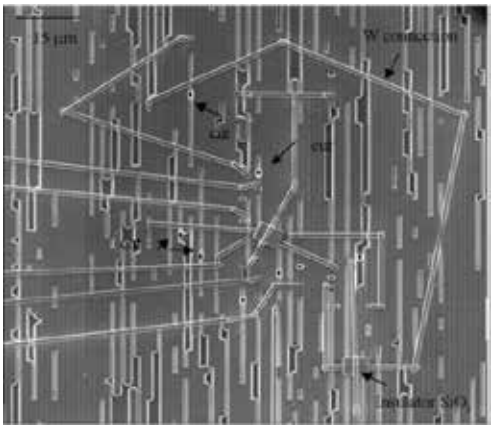

Figure 1: Multiple connections and cuts are shown for front-side FIB circuit edit.

Focused Ion Beam (FIB) Circuit Edit Becomes Increasingly Valuable in High-Stakes World of Advanced Node Design

FIB circuit edit is performed using a finely focused gallium (Ga+) ion beam with nanoscale resolution. It is possible to image, etch and deposit materials on an IC with an extremely high level of precision. By removing and depositing materials, FIB circuit edit enables designers to cut and connect circuitry within the live device, and to create probe points for electrical testing. It is the equivalent of performing microsurgery on IC devices. The high-energy Ga+ beam can mill through conductors or insulators and uses various types of gases to either enhance milling precision or more effectively deposit conductive and dielectric materials. For instance, by using appropriate gas chemistries, a choice of tungsten, platinum or silicon dioxide can be very precisely deposited using the ion beam.

In order to perform circuit edits, the FIB tool is coupled to a CAD navigation system that makes it possible to locate the area of interest. FIB circuit edit typically uses the designer's GDS files as a road map. This provides a method to find subsurface features and ensuring that the right edits are made (see Fig. 2). Accurate beam positioning is one of the most critical requirements for FIB circuit edit. The sample must have some features that the GDS files can be locked into so the stage can drive with the GDS file.

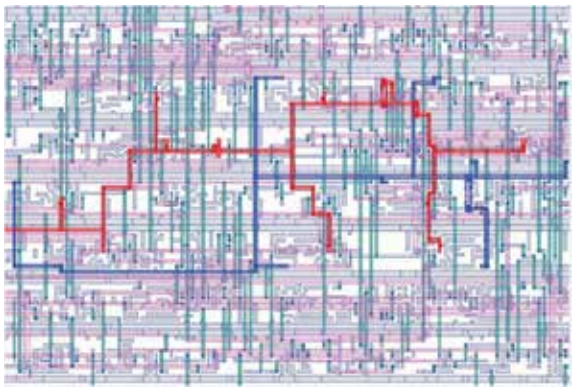

Figure 2: CAD layouts are used to perform FIB circuit edits.

FIB CIRCUIT EDIT APPLICATIONS

There are many uses for FIB circuit edit at every commercially available node. It can be used to verify design change on the tester, the bench via probing, and to validate design change at the system board level.

Typical applications include:

- Debugging and optimizing devices that are already in production – FIB circuit edits are often performed once a design flaw has been identified. This ensures that the proposed fix will resolve the problem. Designers can repair mask errors and know that the device will work after one and not two mask spins, while simultaneously expediting the next steps by getting working prototypes into customers' hands so they can continue software development. As cycle times in mobile device and other market segments become more and more compressed, avoiding a week of lost cycle time can be extremely important for a successful product roll-out.
- Exploring and validating design changes – more than just simulation is required to optimize designs. FIB circuit edit enables designers to try derivatives of device designs and observe the results. They can explore options like cut-away fuses or other functional changes, and experiment with them on a live device before committing to the cost or timetable of a complex mask spin.
- Prototyping new devices without costly and time-consuming mask set fabrication – FIB prototype devices are often used to enable next-level testing. This enables developers to get a jumpstart on the next round of device debug and accelerate design cycles. FIB circuit edit eliminates the need for multiple prototype testing rounds and mask modification cycles. Designers can implement and evaluate the results of circuit changes on physical prototypes that will optimize or correct flaws in the design before committing to them in a new mask spin. What would otherwise cost $5 million to $10 million in wafer costs and 6-8 weeks in wafer processing cycle time can be done for hundreds or thousands of dollars in a matter of hours, ensuring that only one additional wafer spin will be required.
- Duplicating and scaling fixes: Once a fix has been verified on a prototype using FIB circuit edit, it is possible to duplicate that fix on a handful or tens of devices to provide internal test, validation, and qualification teams and even customer samples. By doing this, further system or application development work can then take place in parallel while waiting for the mask spin and final production devices to come back.
- Accelerating time to market: Delivering on time is vitally important to customers. Their product designs are essentially on hold until they can get working devices. FIB circuit edit speeds up the entire cycle. It gets customers into production and avoids loss of reputation, or the risk of competitors getting their foot in the door, etc. Some large OEM customers also impose late-delivery penalties that can reach millions of dollars. Fig. 3 shows the best approach for integrating FIB circuit edit into the overall IC development and testing process

In the power semiconductor arena, most current control products are fabricated using traditional silicon technology, and FIB circuit edit is performed in much the same way with these devices as it is with any other analog or digital circuits. In the future, there is a strong possibility that drivers will move to wide bandgap materials. FIB circuit edit should offer benefits for these devices, as well. SiC, GaN and other wide bandgap semiconductor materials enable power semiconductor devices to withstand high voltages

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Figure 3: FIB circuit edit can be inserted both at the simulation stage and later during de-bug to optimize success rates during the IC design process.

and temperatures, while providing higher frequency response, increased current density and faster switching speeds. At the same time, however, they present complex challenges related to design and characterization, process monitoring and reliability. Challenges become even more difficult at advanced process nodes.

FIB CIRCUIT EDIT TECHNIQUES CONTINUE TO IMPROVE

There is a relatively common misperception that FIB circuit edit only works well at 90nm and 65nm process nodes, and that it has "run out of gas" at smaller nodes. This is simply not true. Thanks to tool and methodology advances that have been derived from the experience of dedicated teams running thousands of circuit edit hours. FIB circuit edit can now be used for more precise beam guidance, operate in smaller areas, perform more intricate operations on both the back and front sides of the device, and handle copper layers. Most of the edits are done on the metal traces and have nothing to do with the gates. The geometry of the area where the cuts and jumps are to be made are all that determine if an alteration can be made.

A major development area for FIB circuit edit is the ability for tools to provide better aspect ratio for smaller cuts. FIB systems continue to deliver greater benefits thanks to advances in areas such as ion beam resolution, operating software and CAD navigation. Ion beam resolution advances, alone, have delivered significant new capabilities that have been critical for recognizing small features, aiding in visual end-pointing, enabling precise CAD alignment, and improving box placement accuracy. Fig. 4 shows resolution advances that have been achieved from 2008 to the present.

Tool advances are only part of the story. Because FIB tools are not entirely automated, there is no under-estimating the critical importance of FIB operator experience to circuit edit success. The process is definitely a mix of science and art. For example, endpoint detection, (or the ability to know when selected layers of interest have been successfully etched through) continues to require a high level of skill in order to achieve high success rates. Operator skill in this area is even more important at smaller geometries. Also important is the unique operator knowledge in areas of IC circuitry, IC process technology, ion milling patterns, and general FIB tool usage.

Achieving this expertise can be difficult for an in-house operation. Often, larger semiconductor companies who already conduct some level of circuit edit will augment these resources with external service labs that have deeper and more extensive experience in solving the toughest FIB circuit edit challenges. As for small- and mid-sized companies, few can bear the expense of purchasing a FIB tool that might cost $1 to $2 million plus the lab, service contracts, and the operators. Even if they could afford the tool, it would be difficult to staff a team with the necessary experience to most effectively operate the system. Most companies of this size tend to go directly to an external lab that can implement circuit edits to support basic electrical design characterization or verification of redesign parameters and offers a full range of debug tools necessary for solving difficult logic failures and other anomalies. The outside service labs can run on extended hours to reduce the costs and do work for many companies; effectively spreading the costs across the industry.

BEST PRACTICES FOR FIB CIRCUIT EDIT

There are numerous prerequisites for FIB circuit edit success, including tools that provide High resolution is particularly important at advanced nodes such as 20 nm and lower. Designs generally require a 0.1um resolution as well as a trenching approach that supports a finer resolution in order to make these edits. The smallest hole that can be made with today's equipment is 0.1 x 0.1 um with an aspect ratio of 20:1. For most 20 nm and 28 nm designs, it is impossible to make a small enough hole to reach the target directly. As a result, specialized FIB techniques are required in order to increase the aspect ratio and gain access to the target. The system must be able to smoothly remove dummy metal above the target metal layer. This also requires deep and extensive knowledge of IC circuitry and processes, FIB tools and ion milling patterns. Figure 5 shows a typical back-side trench.

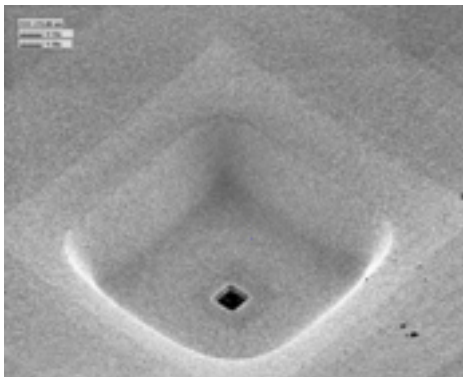

Figure 5: Today's trenching approaches support fine enough resolutions to enable FIB circuit edits at advanced nodes.

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For Backside and frontside editing, many erroneously believe that flip chip FIB circuit edit can only be performed from the top of the device. On the contrary, backside edit is frequently the most effective way to operate on flip chip devices. This is true because of the increased number of metal circuit layers in today's ICs, which makes it harder to reach a lower layer when editing from the top. Fig. 6 shows a back-side FIB circuit edit in which a resistor is introduced across two nodes.

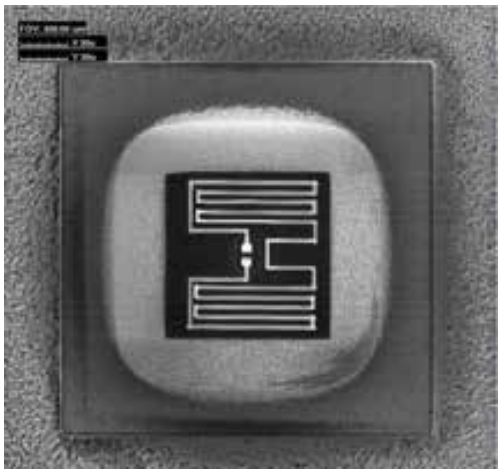

Figure 6: Back-side FIB circuit edit is used to introduce a resistor across two nodes.

In another example, Fig. 7 shows a typical back-side FIB circuit edit in which a probe pad is formed for micro probing. This allows direct probing on the bench. This allows very specific portions of the circuitry to be analyzed.

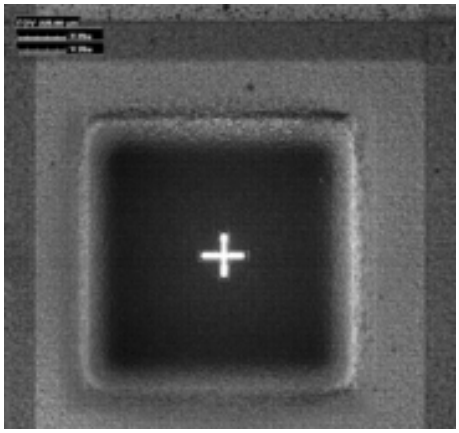

Figure 7: High-resolution trenching enables edits at advanced nodes. [Image courtesy of FIB International Inc.]

When handling copper layers, most 20 nm and smaller node devices are made with copper traces. These devices feature a crystal structure in the copper which is very difficult to remove smoothly. Special methods are required, as well as the tool operator's experience to remove all the copper completely. Also, accurate beam positioning is more challenging for copper metal devices due to the lower visibility of the circuit patterns. This is also important for aluminum metal devices if there are no unique patterns to recognize on the top level.

Companion failure analysis and test tools, expertise and capabilities should also be considered as most devices must ultimately find their way into packages, so that there is a smooth transition to de-capping or de-lidding the devices and performing micro probing and other de-bugging tests on FIB-edited parts.

Front-end expertise is also important as in addition to presenting challenges due to ever-shrinking nano-scale geometrics, semiconductor advanced technology nodes also introduce new front-end materials as processes evolve. FIB circuit edit labs can benefit from being part of a larger lab environment characterized by a significant level of front-end process understanding and materials expertise. Labs that support process R&D activity and yield support will be able to offer an advantage and insights, as well as other know-how that will help maximize the success of FIB circuit edit strategies.

The process of sputtering down to the location of interest in a way that does not cause opens, shorts or leakage is key to the success of circuit edits. The proper strategy coupled with an excellent tool and experienced operator become more necessary as the nodes (geometries) get smaller. An example of this type or work is shown below in the three images: first a large area is opened, then four smaller windows are created in the areas where the editing is to be performed, and lastly the actual cuts and jumper are laid in. These operations can be done on any node, even cutting-edge ones, provided an area with the proper geometries and clearances can be found.

MOORE'S LAW AND SINGLE DIGIT NM CIRCUIT EDIT

As Moore's law continues to accellerate, IC design verification and validation will continue to increase in difficulty as the industry moves down the nano-scale geometry curve. Twenty-eight, twenty nm are common, fourteen is here while seven and nine are in the R&D phase. While some may believe that FIB circuit edit is obsolete at today's advanced nodes, on the contrary it is becoming increasingly valuable for improving the success rates for these designs, which often can cost $10 million or more to bring to market. Due to advances in both tool technology and best practices, FIB circuit edit can be used at advanced nodes for a variety of purposes including debugging and validating fixes, as well as earlier in the process to explore opportunities for design optimization, without having to commit to multiple expensive and time-consuming full mask spin.