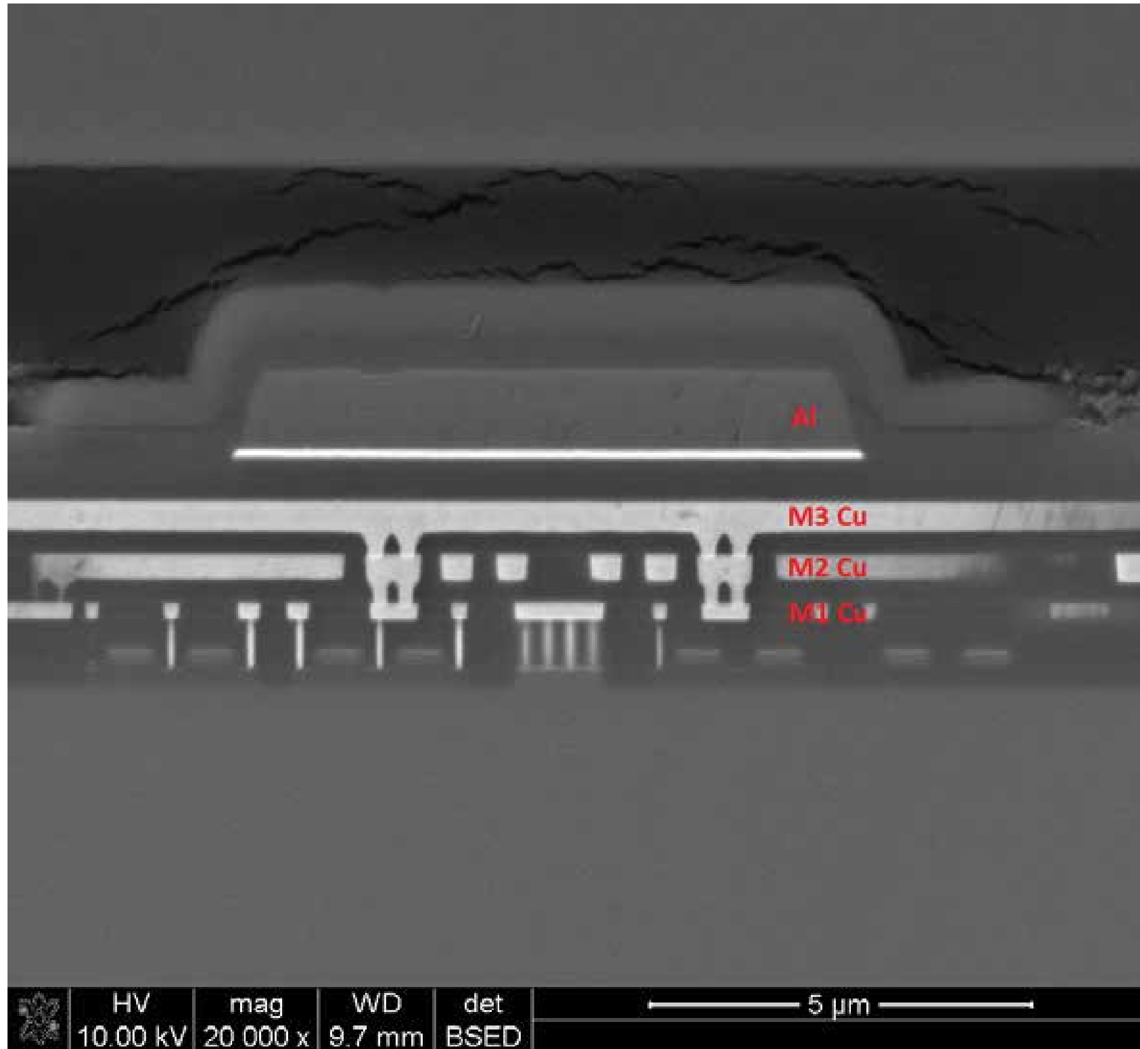
EAG LABORATORIES | Eurofins Engineering Science

PICTURE BOOK

Delayering of Copper Metallization Semiconductor Chips

The process of layer by layer inspection of semiconductor die involves many steps. For failure analysis the area to be inspected must be determined, usually by localization techniques such as emission, hot spot, OBIRCH, or even sometimes optical inspection.

The layer structure must also be known to allow the best methods to be used in the delayering process. Sometimes the layer structure is known, otherwise a mechanical or Dual Beam FIB cross section can be used to directly determine the layer structure as shown below.



Cross section of die

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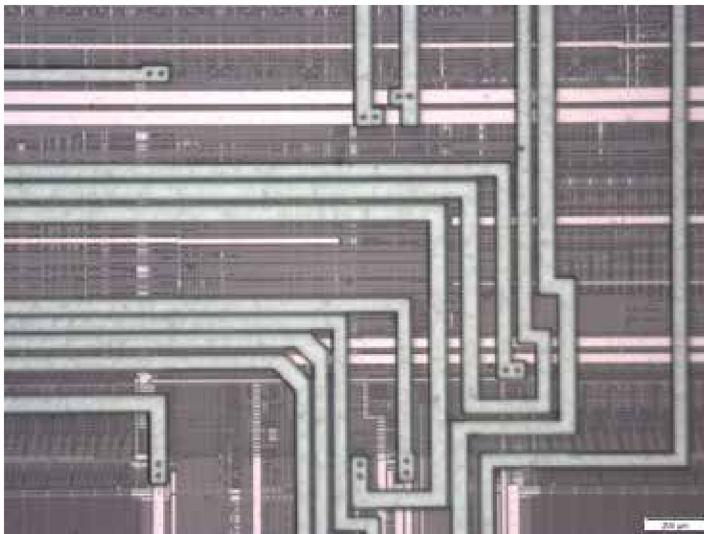
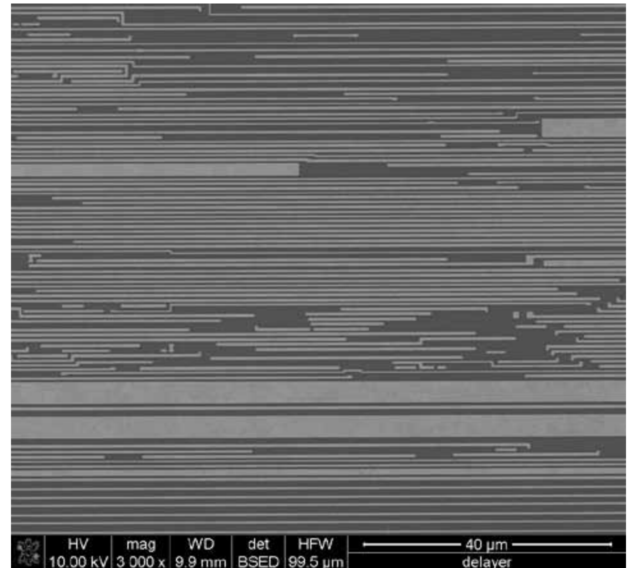
Delayering of Copper Metallization Semiconductor Chips

Once the area of interest is determined, the intact chip is inspected with optical microscopy as shown below.

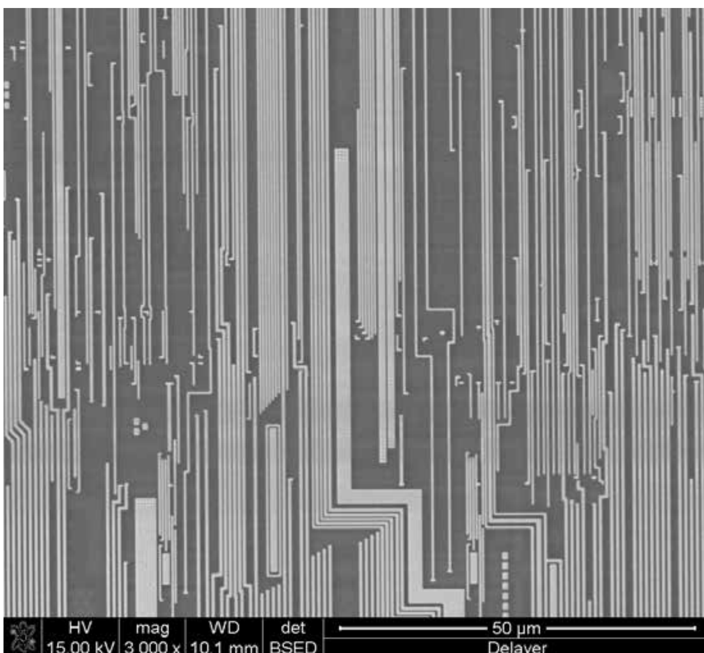


Optical Image Before Delayer

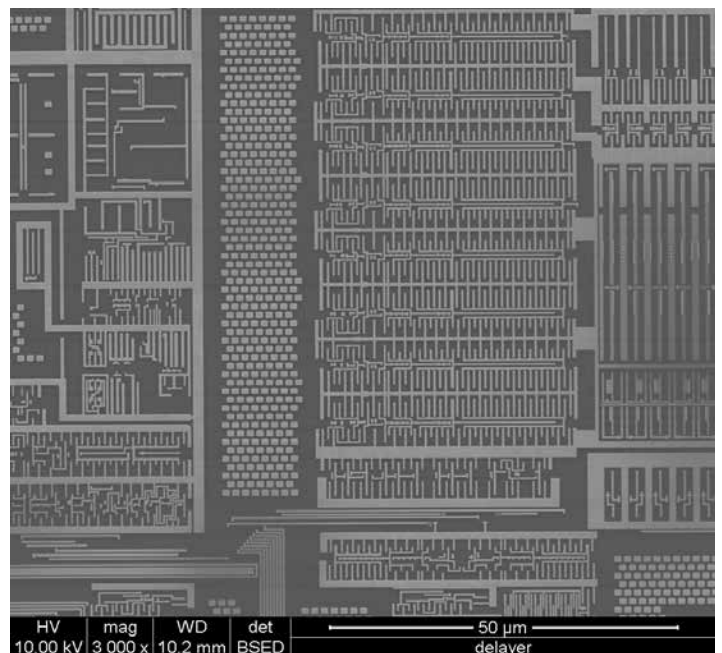


M3

The passivation (glass) is then removed and the next metal layer inspected optically or by SEM (as in the three metal layers shown, and poly and substrate in the next page). If defects are observed then higher magnification images would be taken.



M2



M1

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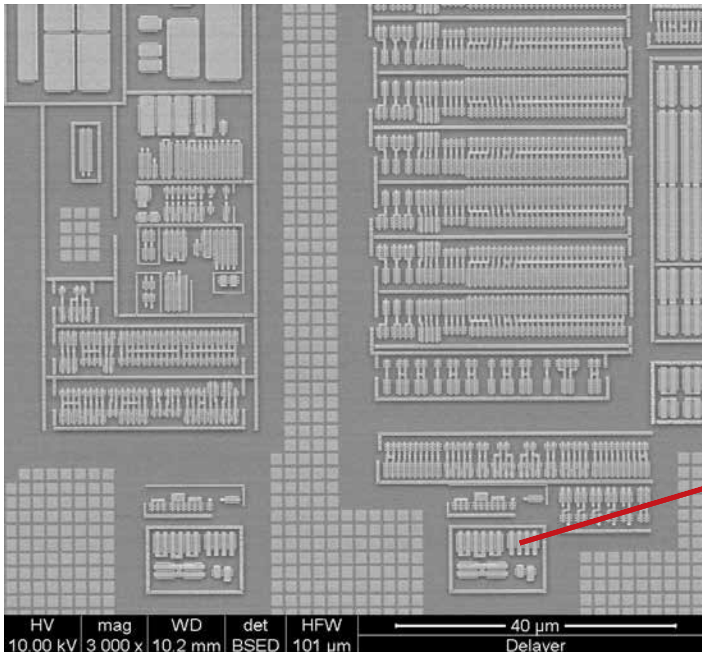
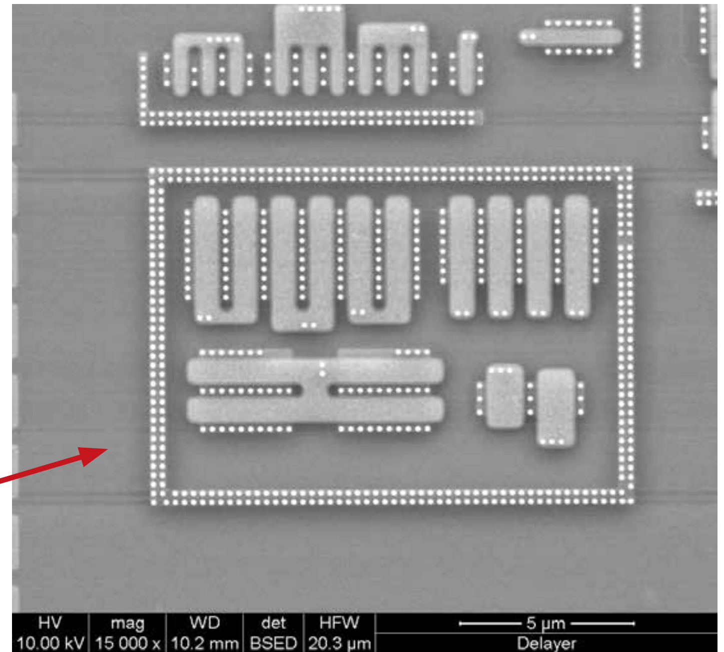
The typical defects observed in each layer are summarized in the table below.

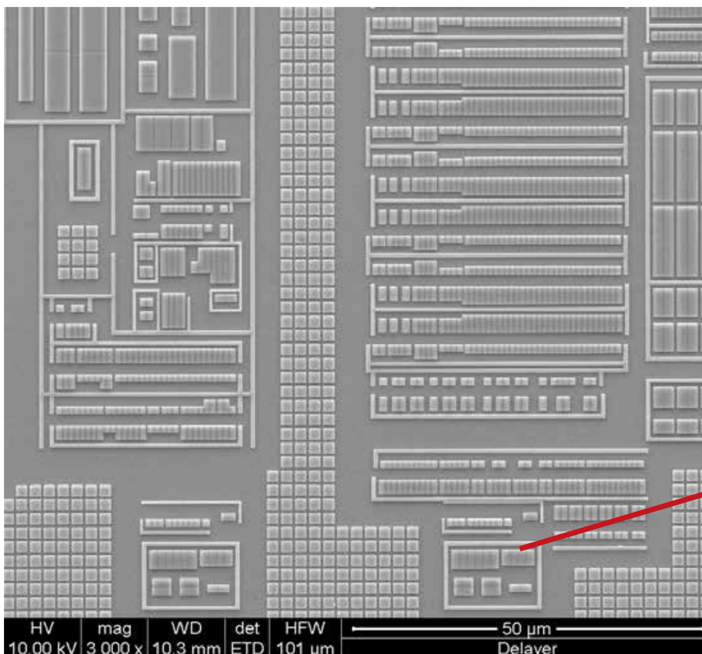
Layers	Typical Defects
Cu Layer	EOS (melting metal), metal short, electromigration, missing via
Contact	PVC (passive voltage contrast) showing leakage or short, missing contact
Polysilicon	Poly short, Tungsten short, missing Poly, missing Silicide
Substrate	ESD damage, melted Silicon, diffusion short, contact spiking, gate oxide defect



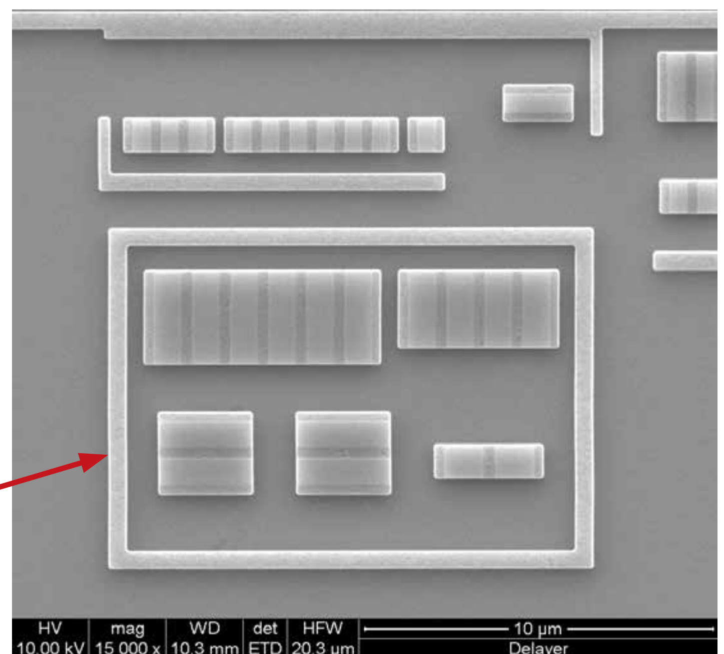
Poly and contact



Poly and contact (high mag)



Substrate



Substrate (high mag)

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