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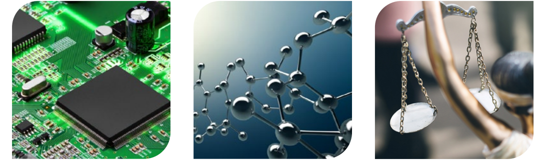


APPLICATION NOTE

Single digit nm Circuit Edit

Pushing the limits to assist Advanced Node Design

Many experts in our industry believe that Circuit Edit using a Focused Ion Beam is no longer feasible for process nodes below 20nm. EAG Laboratories has been able to assist our customers with Circuit Edits on geometries at the single digit nanometer scale. With the rising cost of the development of devices at advanced nodes reaching over $10 million, this Application Note will discuss the typical uses and how our engineers push the limits of this technique to allow early correction of any device errors, and also allow for the ability to generate hundreds of edited samples for customer demonstrations, and continued development and engineering test.

How does FIB Circuit Edit work?

Like an experienced surgeon, it takes both skill and a tuned precision tool to perform these nanoscale incisions on an IC device.
FIB circuit edit is performed using a finely focused gallium (Ga+) ion beam with nanoscale resolution (see Fig. 1). It is possible to image, etch and deposit materials on an IC with an extremely high level of precision. By removing and depositing materials, FIB circuit edit enables designers to cut and connect circuitry within the live device, and to create probe points for electrical testing.

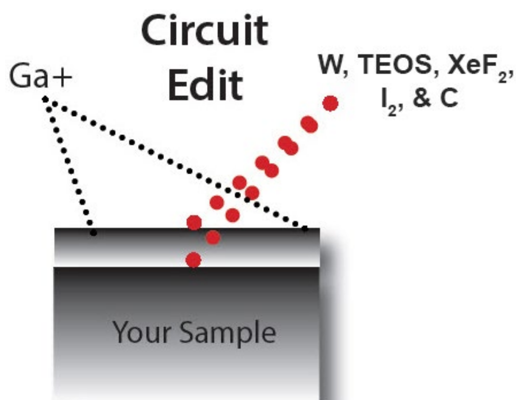
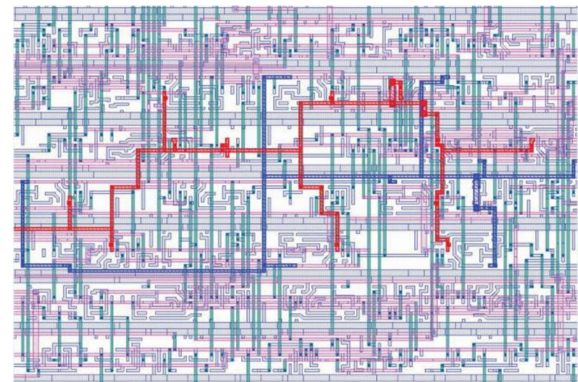


Fig. 1: Typical FIB configuration

The high-energy Ga+ beam can mill through conductors or insulators and uses various types of gases to either enhance milling precision or more effectively deposit conductive and dielectric materials.
Using appropriate gas chemistries, a choice of tungsten, platinum or silicon dioxide can be very precisely deposited using the ion beam.
In order to perform circuit edits, the FIB tool is coupled to a CAD navigation system (see Fig. 2) that makes it possible to locate the area of interest.



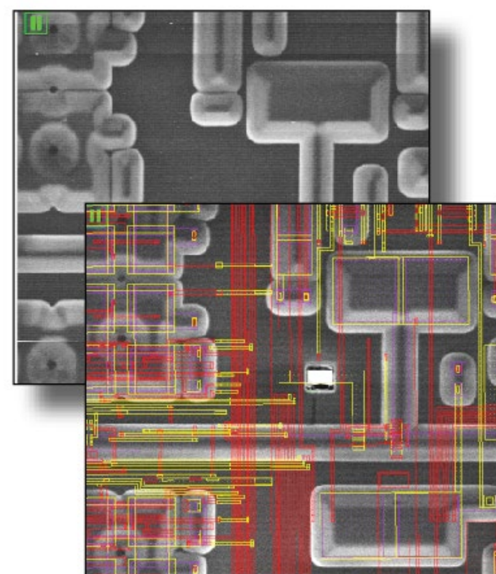


Fig. 2: Examples showing a CAD navigation pattern is overlaid onto an ion generated image

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FIB circuit edit typically uses the designer's GDS files as a road map. This provides a method to find subsurface features and ensuring that the right edits are made Accurate beam positioning is one of the most critical requirements for FIB circuit edit. The sample must have some features that the GDS files can be locked into so the stage can drive with the GDS file.

Typical FIB Circuit Edit Applications

FIB systems allow the semiconductor industry to edit circuits by allowing designers to cut traces or add metal connections within a chip (see Fig. 1).

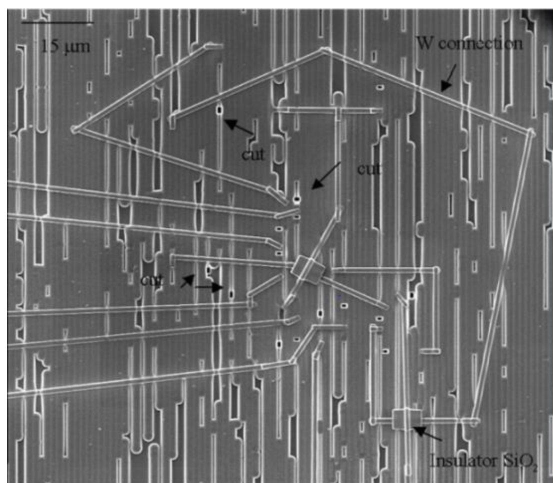

Figure 1: Multiple connections and cuts are shown for front-side FIB circuit edit.

There are many places to utilize FIB circuit edit. It can be used to verify design change on the tester, the bench via probing, and to validate design change at the system board level. Fig. 3 shows entry points for integrating FIB circuit edit into the overall IC development and testing process. The following section highlights typical applications.

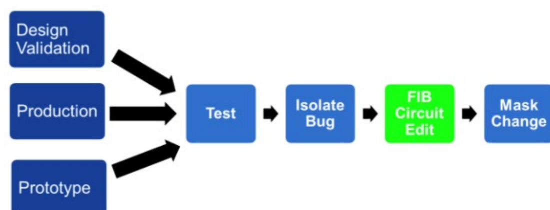

Figure 3: FIB circuit edit can be inserted both at the simulation stage and later during de-bug to optimize success rates during the IC design process.

Debugging and optimizing devices

When a design flaw has been identified, FIB circuit edits can ensure that the proposed fix will resolve the problem. Designers can repair mask errors to determine if the device will work with only one mask spin and it allows prototypes to continue to the software development team. As cycle times become more compressed, avoiding even a week of lost development can be extremely important for a successful product roll-out.

Exploring and validating design changes

FIB circuit edit enables designers to try derivatives of device designs and observe the results. They can explore options like cut-away fuses or other functional changes, and experiment on a live device rather than rely just on simulation before committing to the cost or timetable of a complex mask spin.

Prototyping new devices without costly and time-consuming mask set fabrication

Developers to get a jumpstart on the next round of device debug and accelerate design cycles by using FIB Circuit Edit. Designers can implement and evaluate the results of circuit changes on physical prototypes that will optimize or correct flaws in the design before committing to them in a new mask spin.

Duplicating and scaling fixes

Once a FIB circuit edit fix has been verified on the prototype. It is possible to duplicate the fix on hundreds of additional devices to provide samples to internal test, validation, qualification teams and customers.

FIB Circuit Edit techniques continue to improve

A common misperception is that FIB circuit edit only works well at 90nm and 65nm process nodes. However, tool and methodology advances that have been derived from the experience of dedicated teams running thousands of circuit edit hours has resulted in more precise beam guidance, that can operate in smaller areas, perform more intricate operations on both the back and front sides of the device, and handle copper layers.

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A major development area for FIB circuit edit is the ability for tools to provide better aspect ratio for smaller cuts. FIB systems continue to deliver greater benefits thanks to advances in areas such as ion beam resolution, operating software and CAD navigation. Ion beam resolution advances have delivered significant new capabilities that have been critical for recognizing small features, aiding in visual end-pointing, enabling precise CAD alignment, and improving box placement accuracy. Fig. 4 shows resolution advances that have been achieved since 2008.

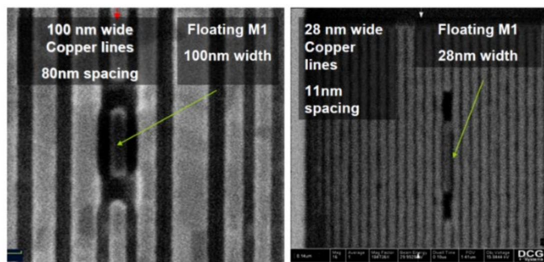

Figure 4 The image on the left shows bit lines on a 90nm process in 2008, while the image on the right shows the bit line for a sub-25nm device today. [photo courtesy of FEI)

Tool advances are only part of the story. Because FIB tools are not entirely automated, there is no under-estimating the critical importance of FIB operator experience to circuit edit success. For example, endpoint detection, (or the ability to know when selected layers of interest have been successfully etched through) requires a high level of skill coupled with knowledge in areas of IC circuitry, IC process technology, ion milling patterns, and general FIB tool usage.

Best practices for FIB Circuit Edit

There are numerous prerequisites for FIB circuit edit success, including:

- Tools: High resolution is particularly important at advanced nodes such as 20 nm and lower. Designs generally require a 0.1um resolution as well as a trenching approach that supports a finer resolution in order to make these edits. The smallest hole that can be made with today's equipment is 0.1 x 0.1 um with an aspect ratio of 20:1. For most 20 nm and 28 nm designs, it is impossible to make a small enough hole to reach the target directly. As a result, specialized FIB techniques are required in order to increase the aspect ratio and gain access to the target. The system must be able to smoothly remove dummy metal above the target metal layer. This also requires deep and extensive knowledge of IC circuitry and processes, FIB tools and ion milling patterns. Figure 5 shows a typical back-side trench.

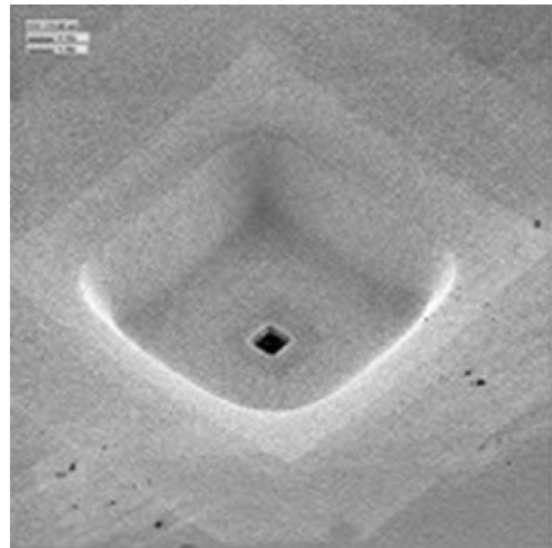

Figure 5: Today's trenching approaches support fine enough resolutions to enable FIB circuit edits at advanced nodes.

- Backside and frontside editing: Many erroneously believe that flip chip FIB circuit edit can only be performed from the top of the device. On the contrary, backside edit is frequently the most effective way to operate on flip chip devices. This is true because of the increased number of metal circuit layers in today's ICs, which makes it harder to reach a lower layer when editing from the top. Fig. 6 shows a back-side FIB circuit edit in which a resistor is introduced across two nodes.

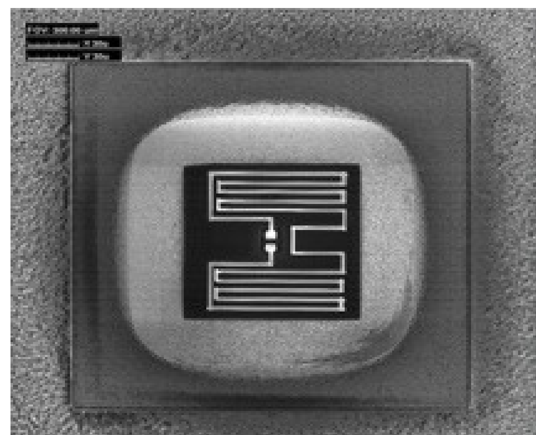

Figure 6: Back-side FIB circuit edit is used to introduce a resistor across two nodes.

- In another example, Fig. 7 shows a typical back-side FIB circuit edit in which a probe pad is formed for micro probing. This allows direct probing on the bench. This allows very specific portions of the circuitry to be analyzed.

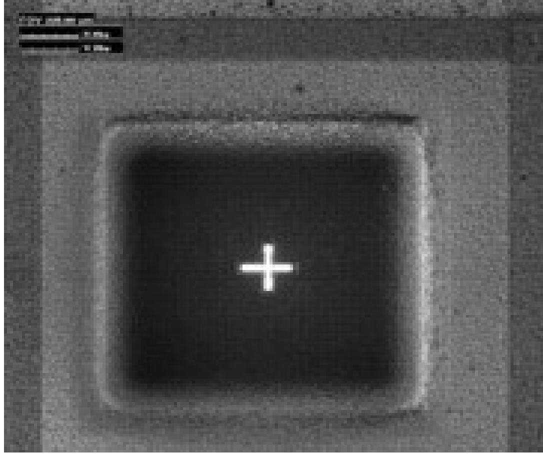

Figure 7: High-resolution trenching enables edits at advanced nodes. [Image courtesy of FIB International Inc.]

- Handling copper layers: Most 20 nm and smaller node devices are made with copper traces. These devices feature a crystal structure in the copper which is very difficult to remove smoothly. Special methods are required, as well as the tool operator's experience to remove all the copper completely. Also, accurate beam positioning is more challenging for copper metal devices due to the lower visibility of the circuit patterns. This is also important for aluminum metal devices if there are no unique patterns to recognize on the top level.

- Companion failure analysis and test tools, expertise and capabilities: Because most devices must ultimately find their way into packages, there should be a smooth transition to de-capping or de-lidding the devices and performing micro probing and other de-bugging tests on FIB-edited parts.

- Front-end expertise: In addition to presenting challenges due to ever-shrinking nano-scale geometrics, semiconductor advanced technology nodes also introduce new front-end materials as processes evolve. FIB circuit edit labs can benefit from being part of a larger lab environment characterized by a significant level of front-end process understanding and materials expertise. Labs that support process R&D activity and yield support will be able to offer an advantage and insights, as well as other know-how that will help maximize the success of FIB circuit edit strategies.

- The process of sputtering down to the location of interest in a way that does not cause opens, shorts or leakage is key to the success of circuit edits. The proper strategy coupled with an excellent tool and experienced operator become more necessary as the nodes (geometries) get smaller. An example of this type or work is shown below in the three images shown in Fig. 8, 9, & 10. These operations can be done on any node, even cutting-edge ones, provided an area with the proper geometries and clearances can be found.

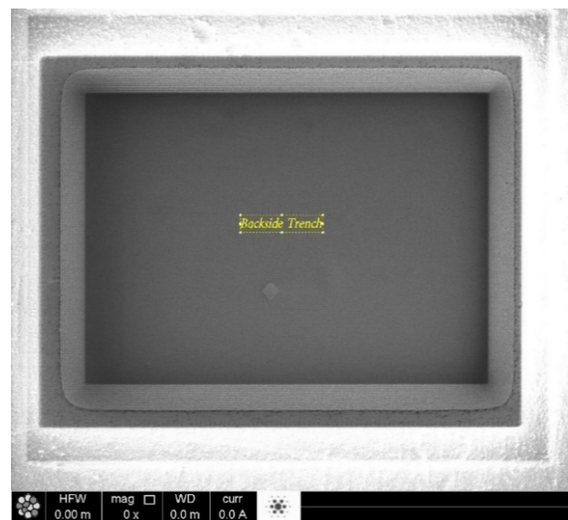

Figure 8: A large area is opened.

Figure 9: Four smaller windows are created in the areas where the editing is to be performed.

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Figure 10: The actual cuts and jumper are laid

Accelerating time to market

Delivering on time is vitally important to customers as designs are on hold until they can validate working devices. FIB circuit edit allows devices to go into production quicker and avoids late-delivery penalties that can reach millions of dollars.
In the power semiconductor arena, IC designers will encounter many new issues as power devices move to silicon carbide (SiC), and Gallium Nitride (GaN) and other wide bandgap semiconductor materials that enable power semiconductor devices to withstand high voltages and temperatures, while providing higher frequency response, increased current density and faster switching speeds. Due to the increased complexity and cost of manufacturing these devices, FIB Circuit Edit has proven to be a useful tool to reduce costs and improve the time to market.

Advanced Process Nodes

Designers encounter many new challenges at advanced process nodes as the mask costs are high, and it is much more difficult to find and fix bugs. As the complexity of the design increases, the simulation times are growing, and many designs simply cannot be 100 percent verified without physical samples. Simulation models may be imperfect for complex designs and packaging can cause stresses to sensitive devices. The need to verify the final product and make changes to improve/fix designs will remain in play. Challenges in this environment range from multiple patterning and layout dependent effects (LDE) to the use of local interconnect layers. Design and integration complexity give rise to a new level of difficulty with each new technology node. Fast signals and high power electromigration also create challenges. Decreasing metal pitch leads to coupling effects and signal integrity issues. Increasing wire and via resistance requires more advanced and variable wire sizing and tapering techniques. Additionally, extraction, timing, signal integrity analysis, and modeling pose a multitude of issues that designers must solve before they can achieve the required accuracy on a new device. This often requires a check on a physical sample and the CE FIB allows alteration of the sample to check results from changes in the layout.

Single digit nm Circuit Edit

IC design verification and validation has continued to increase in difficulty as the industry moves down the nano-scale geometry curve. While some may believe that FIB circuit edit is obsolete at today's advanced nodes, due to advances in both tool technology and best practices, EAG Laboratories has successfully performed Circuit Edits at the 7nm scale for customers that are in the R&D phase.
What would otherwise cost $5 million to $10 million in wafer costs and 6-8 weeks in wafer processing cycle time can be done for hundreds or thousands of dollars in a matter of hours, ensuring that only one additional wafer spin will be required.

Also, the ability to generate hundreds of these edited samples allows for customer demonstrations, and additional engineering tests to be continued without delays.

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