Eurofins
Materials Science

APPLICATION NOTE

# Material structural analysis power of PED at nanometer scale

## INTRODUCTION

As the new technologies continue to progress in recent years, materials characterization for such devices and processes becomes ever more challenging. Materials characterization, including chemical/elemental analysis and structural analysis, needs to be performed not only at higher sensitivity but also at much smaller scale. For structural analysis, traditional XRD and SEM based EBSD has been providing materials structural information with great precision. However, until recently, the emerging TEM based Precession Electron Diffraction (PED) technique has started bringing this analysis to the nanometer scale, which has been essential to meet the demand of the nano-scale structural analysis at the nowadays aggressively size-shrinking technologies and processes.

In this application note, examples of crystal grain orientation mapping and strain mapping in various devices (7nm EUV technology IC chip and strained Si) are shown to exemplify the material structural analysis power of PED technique at nanometer scale.

## NANO-SCALE GRAIN ORIENTATION AND GRAIN SIZE ANALYSIS OF METAL LINE IN IC CHIP

In the past a few decades, the semiconductor technology node / transistor size has been decreasing. However, for metal interconnect lines that carry the current/signal, as the metal line size decreases, the resistance increases, leading to more heat and bigger power consumption. Especially, the size of metal lines has shrunk to tens of nanometer recently, and thus the problem becomes much more severe. Several approaches have been proposed to mitigate the problem. One of the them is to manipulate the grain size of the metal line, as the electron tend to scatter at grain boundary leading to resistance. However, characterizing and direct observation of

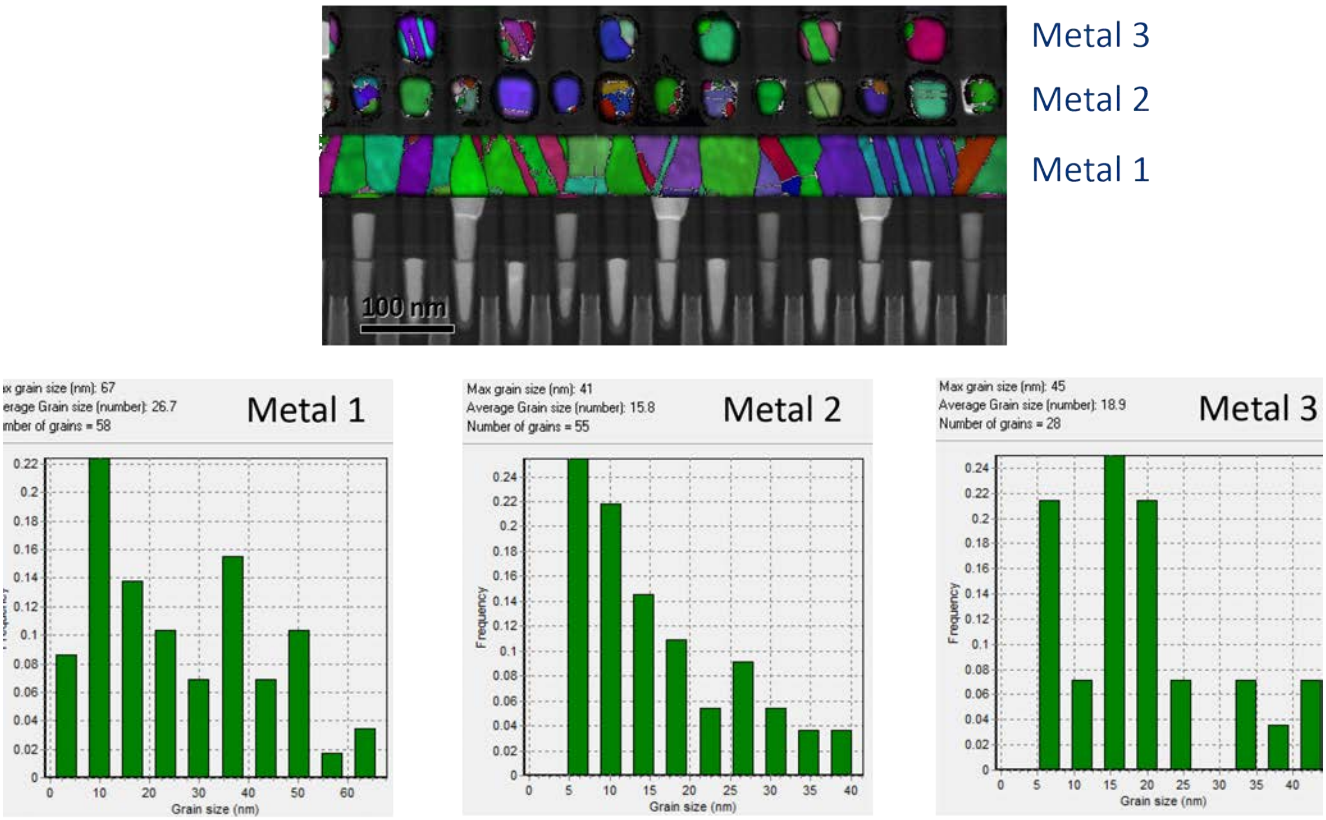


**Figure 1: Grain size distribution of different metal lines of 7nm System On a Chip (SOC) application processor from a smart phone by PED**

# Material structural analysis power of PED at nanometer scale

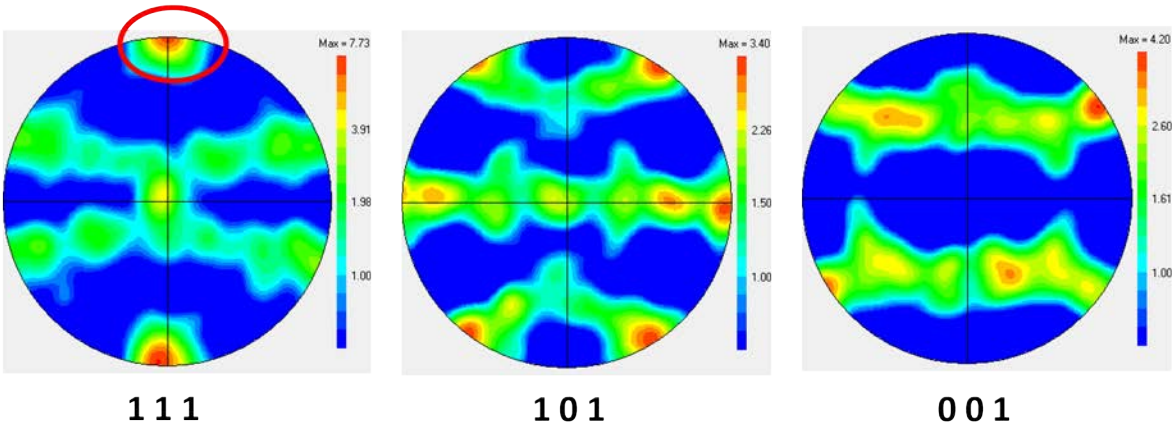


**Figure 2: Pole figure of metal line (Cu)**

the grain size at nanometer scale has been challenging until now due to the resolution limit by other techniques, e.g. EBSD. And here is how PED can help to characterize grain size at nm scale of different metal lines (Fig. 1).

Beside the grain size and grain orientation mapping, PED can also provide statistical quantification of the preferential growth direction (or called texture information) of the metal lines. Using pole figure, whether the grain has preferential growth direction or not can be accessed. In this case, the Cu <111> direction (Fig. 2) has preferential vertical growth direction, shown here in red cycle. This direction is 7 times higher than average direction, which is considered statistically significant.

## NANO-SCALE STRAIN ANALYSIS OF STRAINED SI

The speed that an IC chip can compute and process the data greatly depends on how fast the basic building blocks of the chip – transistor can switch on and off or how fast the signal can pass through the gate. By squeezing the Si lattice or in the other word introducing strain inside Si, the hole – the charge carrier of PMOS can move faster and hence increase the transistor speed. And how to characterize this small strain at nanometer scale is challenging until now. Fig 3. shows strained level in 45nm techonlogy node transistor with high sensitivity and high resolution by PED.

## SUMMARY

Besides the early success in solving materials structure with XRD and SEM-based EBSD, it was only until recently with the commercial availability of TEM based PED technique that direct observation of materials structure at nanometer scale has become possible. Novel applications of PED include crystal grain orientation, grain size distribution, texture information, grain boundary analysis, strain mapping at nanometer scale on various crystalline materials.

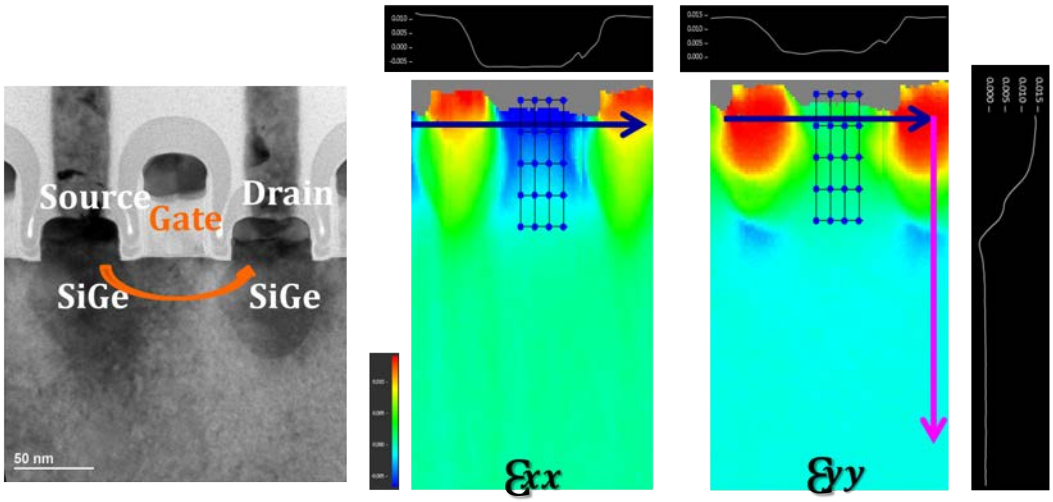


**Figure 3: Shows strain mapping of 45nm technology node transistor**