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APPLICATION NOTE

A materials analysis study into FinFET technology advancement: 22 nm to 7 nm

INTRODUCTION

7 nm FinFET (Fin Field Emission Transistor) process technology was introduced to semiconductor manufacturing mass production in 2018, following 10 nm node in 2016, 14 nm node in 2014 and 22 nm node in 2012[1]. While the naming of process nodes is not directly related to any measurable distance on a chip, 7 nm process technology provides shrink down transistors and thus offers improvement in silicon area utilization and power efficiency. In this application note, we provide a materials analysis study into the comparison between 22 nm node and 7 nm node FinFET technologies, using TEM-based (Transmission Electron Microscopy) techniques.

Figure 1 shows HAADF-STEM (High Angle Annual Dark Field – Scanning Transmission Electron Microscope) images of Fin-cut FinFET structures. Figures a-c represents 22 nm node, 14/16 nm node, and 7 nm node, respectively. All of them show Si fin buried in metal gate, with different fin width, height, pitch distances and other critical dimensions (CD). The pitch distance has been significantly reduced from 61.1 nm in 22 nm node, to 55.5 nm in 14/16 nm node, then 30.2 nm in 7 nm node. As a result, 7 nm provides a 3.38X density improvement compared to 14/16 nm (1/(30.2/55.5)^2), which corresponds to Gartner's estimation of 3.3X[2].

Figure 2 shows HRSTEM and HRTEM images of the top region of Fin. Si atom dumbbell of 0.13 nm separation distance is clearly seen in the HRSTEM image. Compared to 22 nm node [3], 7 nm gate oxide is slightly thicker (0.91 nm vs 0.73 nm), while the Fin width is decreased. It is also interesting to see a discontinuity of metal gate layer at top of the Fin tip.

Figure 3 shows elemental distribution of the 7 nm Fin, acquired by TEM-based EELS (Electron Energy Loss Spectroscopy). Sub-nanometer layer of high-k dielectric HfOx is seen, similar to that in 22 nm[3]. However, compared to 22 nm Fin, W from metal contact and Ta in TaN dielectric layer are missing.

To better understand elemental distribution in 7 nm FinFET, gate-cut TEM sample was prepared. Figure 4 reveals EELS mapping results. It is seen that Ta concentration is very low and is non-uniformly distributed. The Fin-cut sample happened to be selected from a Ta-free region. For metal contact, W has been replaced by Co. As metal contact dimension continues to shrink, W causes issues in gap fill and increases contact resistance. Current metal contact seed region is around 8 nm, which exceeds the limit for good W fill, which is 12 nm, thus explains the disappearance of W in 7 nm node. Co offers inherently superior resistance at small dimensions, as a result it is selected as latest FinFET metal contact material [4].

Contact resistance is strongly affected by the sheet resistance of contact metal silicide, thus it is of essential importance to understand metal silicide distribution at the S/D. In FinFET, a commonly-used silicide is TiSi. However, one would encounter

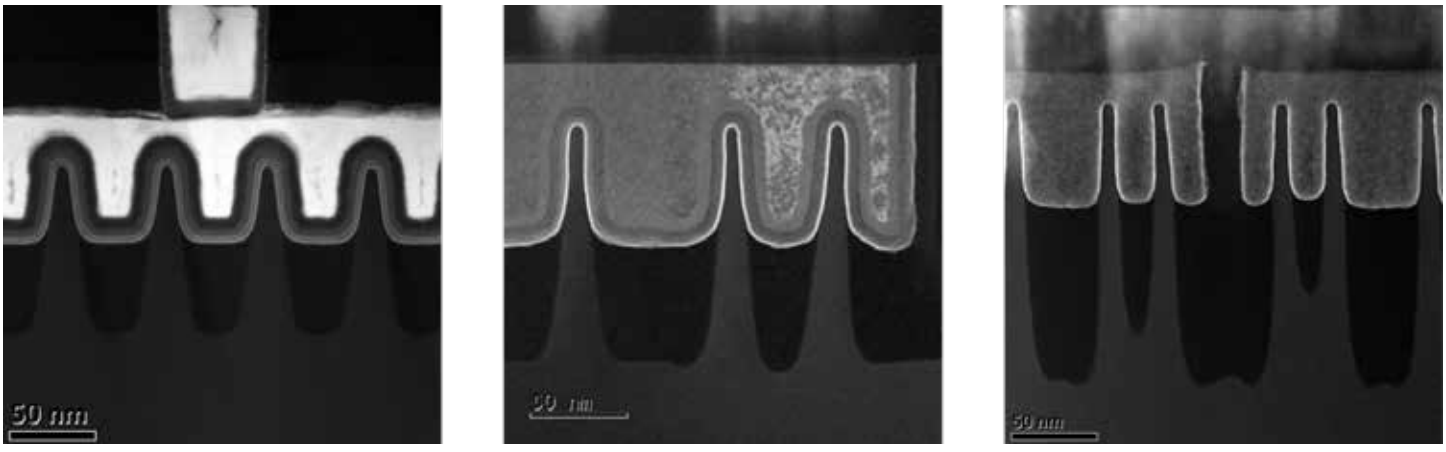

Figure 1: HAADF-STEM images of Fin-cut FinFET; a: 22 nm; b: 14/16 nm; c: 7 nm

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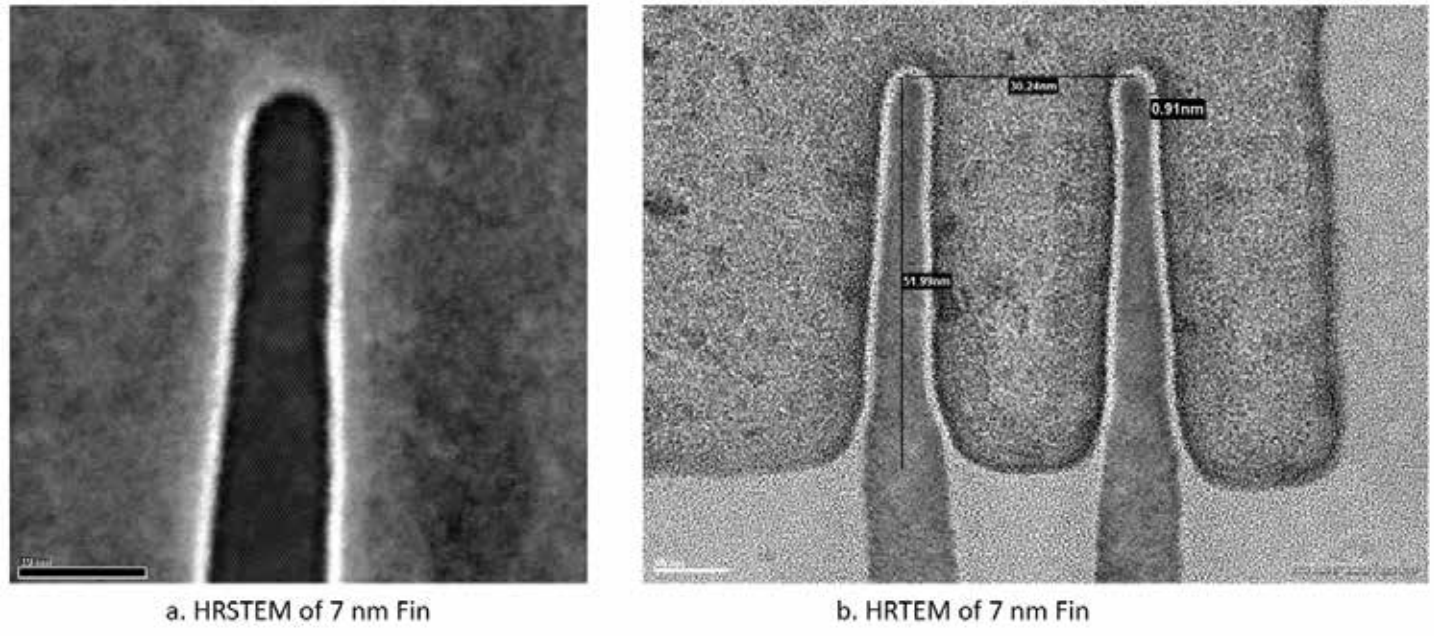

Figure 2: High-Resolution STEM and TEM images of 7 nm Fin

issues while trying to analyze Ti distribution near contact, as the Ti from TiSi is not distinguishable from Ti from TiN barrier layer. We applied EELS to resolve this issue. In Ti L edge EELS spectrum, Ti from TiSi exhibits a shift to the left of ~1-2 eV in comparison to Ti from TiN. Such difference was used to perform multi-linear least square fitting for either kind of Ti, to analyze their respective distribution as TiN and TiSi, as shown in figure 5.

7 nm FinFET still employs Cu metal line. The Cu grain size and orientation preference is analyzed using PED (Precession Electron Diffraction) technique, and the result is shown as figure 6. The M0 Cu average size is 26.7 nm. Compared to 20.7 nm in 22 nm node [3], current grain size is increased by 30%, leading to reduction of grain boundary and heat generation.

REFERENCES

[1]. https://en.wikipedia.org/wiki/7_nm_process

[2]. https://semiengineering.com/10nm-versus-7nm/

[3]. 22 nm FinFET application note

[4]. https://semiengineering.com/dealing-with-resistance-in-chips/

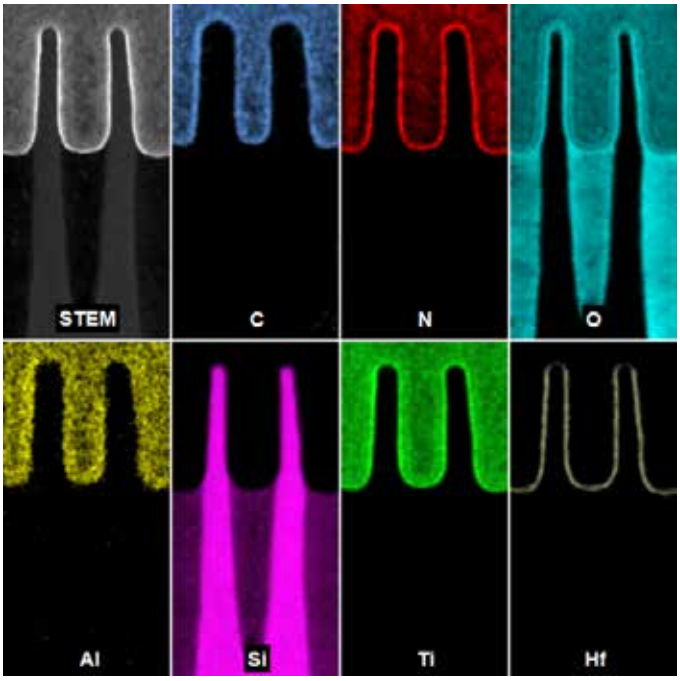

Figure 3. Elemental distribution of 7 nm Fin acquired by EELS

A materials analysis study into FinFET technology advancement: 22 nm to 7 nm

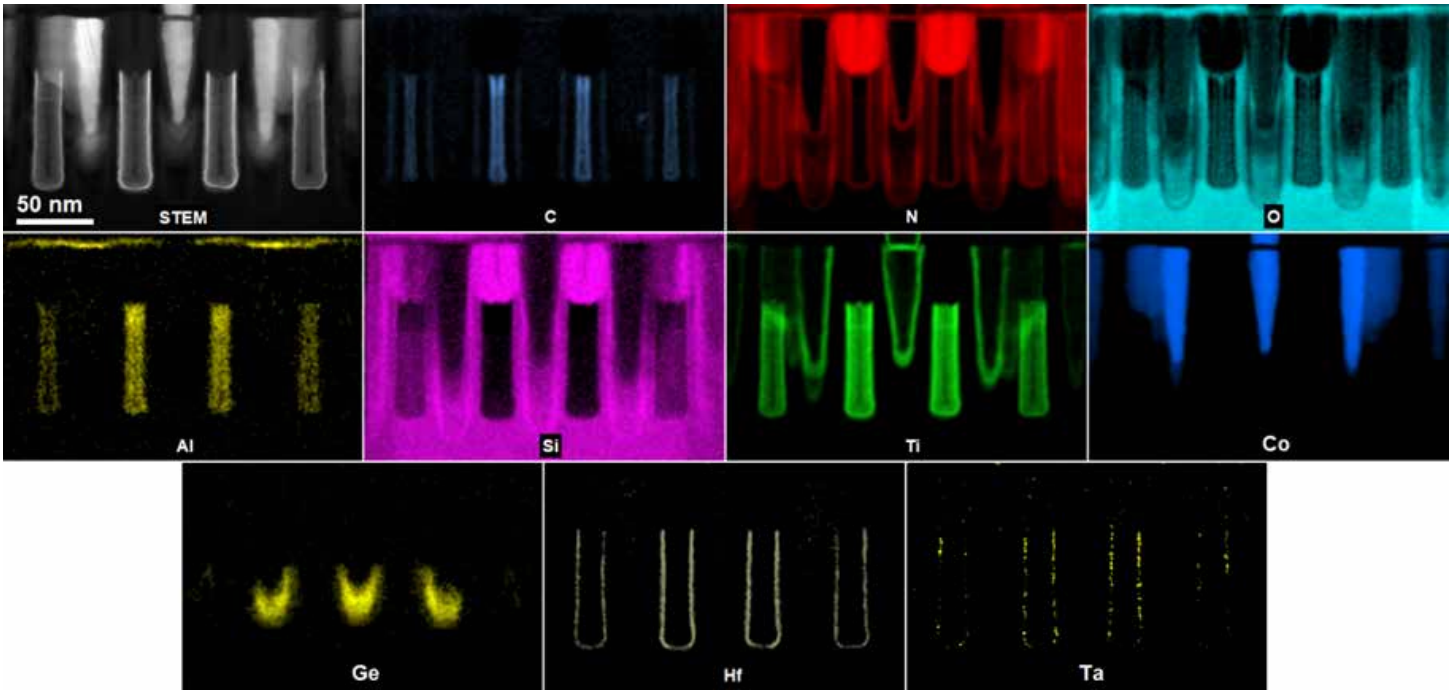

Figure 4: Elemental distribution of 7 nm Fin acquired by EELS, from gate-cut direction

A materials analysis study into FinFET technology advancement: 22 nm to 7 nm

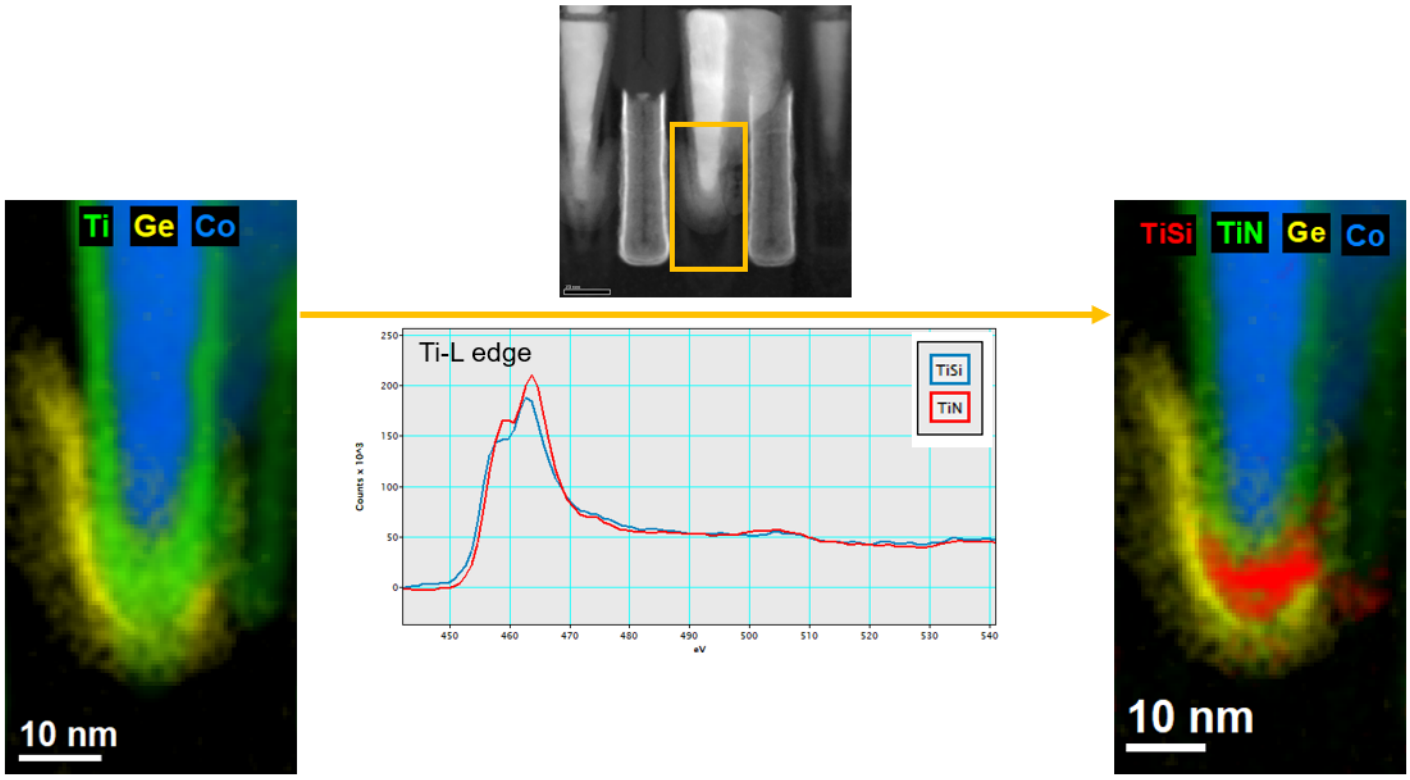

Figure 5. Titanium distribution near metal contact and S/D