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Process to Successfully Perform Dye & Pry of CSP Devices

Chip Scale Packages (CSPs) have been around since the early 1990's. In CSP design, the chip is almost the same size as the substrate. This saves room, but can increase the difficulty of failure analysis including the Dye & Pry process.

The ability to examine solder attachment of a device to a PCB is a very helpful way to quickly evaluate the attach process.

This process is common for other types of mold compound devices, but CSPs tend to be much more brittle and delicate. We have found that the common method of Dye & Pry can result in the cracking and shattering of the die.

The standard process involves cleaning the device that is described in the Dell papers; Dell EMC Dye and Pry Procedure REL0164 Rev A05, IPC-TM-650 2.4.53 Dye and Pull Test Method, & IPC-7095C Design and Assembly Process Implementations for BGAs.

Figure 1. Microscopic examination of board.

Dye & Pry includes a microscopic examination of board where items such as serial number, identification, lot number, or date codes are captured (figure 1).

We inspect using the provided Accept/Reject Criteria in Appendix A-4 (pg7, Dell EMC REL0164 Rev. A05) and an x-ray is used to examine for any anomalies.

The sample is then cleaned to remove any flux residue from around the solder joints. After cleaning, the device is dyed and then pried to break the solder attachment. Both sides are examined by optical microscopy to observe all the solder attach points. A rating system from the Dell paper is applied to characterize the quality of the solder attachment.

However, this standard method can result in the die breaking in multiple locations with some pieces of the die remaining on the substrate side and some lifting off as shown in Figure 2 and 3.

Figure 2. Top down optical with ring lighting on the PCB substrate.

Figure 3. Top down optical with ring lightng on the component substrate.

EAG has altered the common Dye & Pry method, which has resulted in a significantly improved rate of success compared with the standard method.

The results of this new process are shown in Figures 4, 5, and 6.

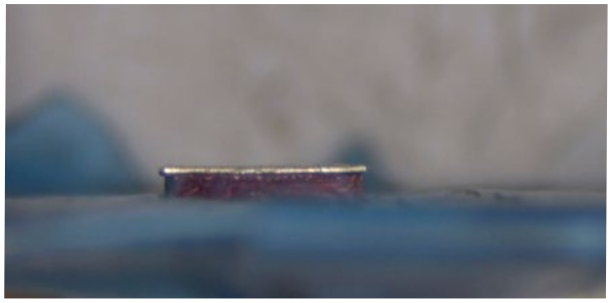

Figure 4. Optical side view of new Dye & Pry process.

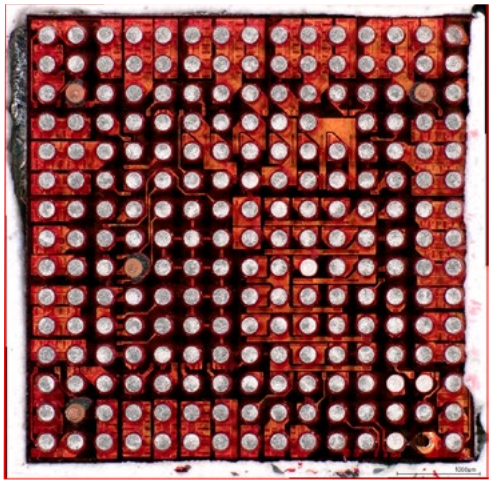

Figure 5. Top down optical with ring lighting of PCB substrate (CSP package) post Dye and Pry.

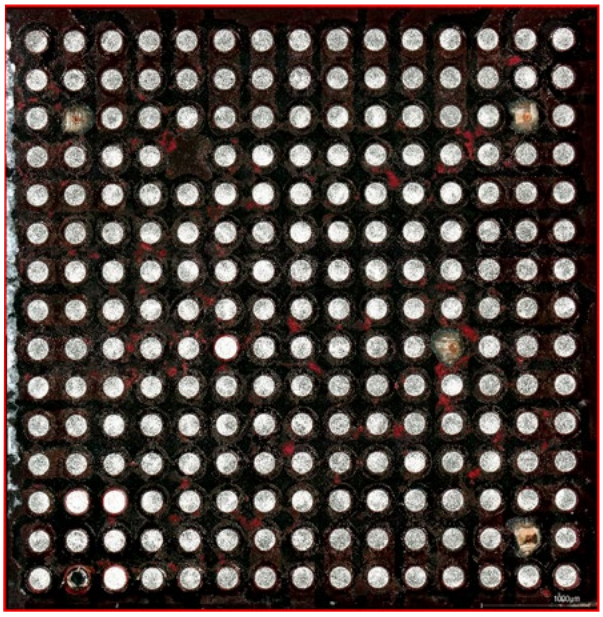

Figure 6. Top down optical with ring lighting of PCB substrate (CSP package) post Dye and Pry.

This process improvement enables us to offer CSP Dye & Pry services that were not previously possible due to the die breakage and incompleteness of the observable area on the device post pry. The device may also be electrically tested on the bench, and this can then continue on to a full failure analysis of the CSP device. In addition, the clean removal of the CSP device also allows for continued Failure Analysis on the PCB.

Dye & Pry is a technique that may assist in failure analysis of Chip Scale Packages, but the EAG team will also provide advice and alternative techniques such as Cross-section, SAM, and X-ray analysis.

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