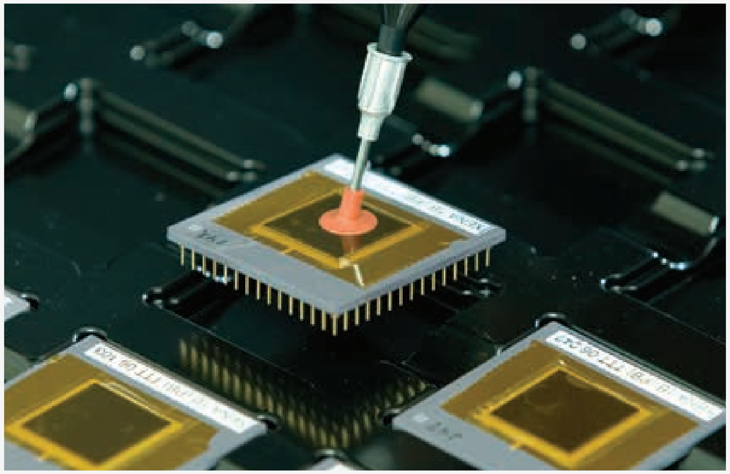

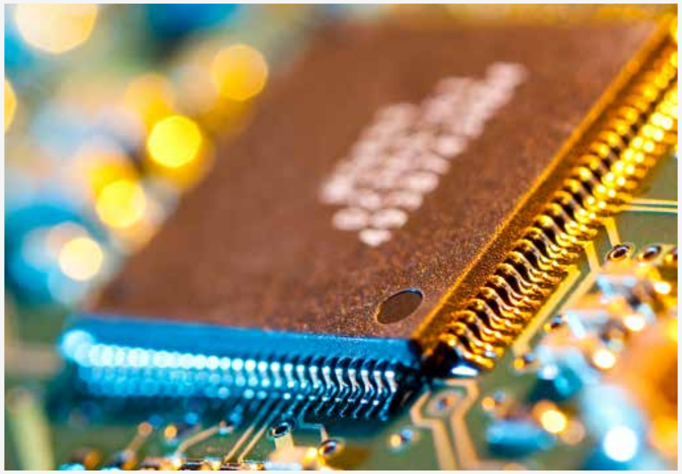

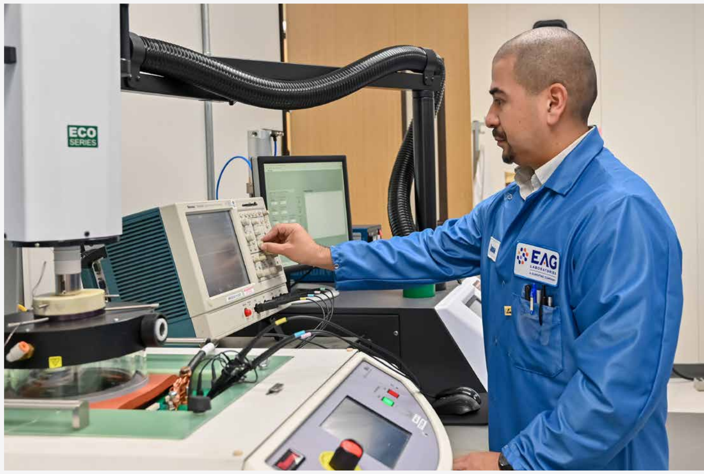

YOUR TRUSTED PARTNER FOR ESD & LATCH-UP TESTING

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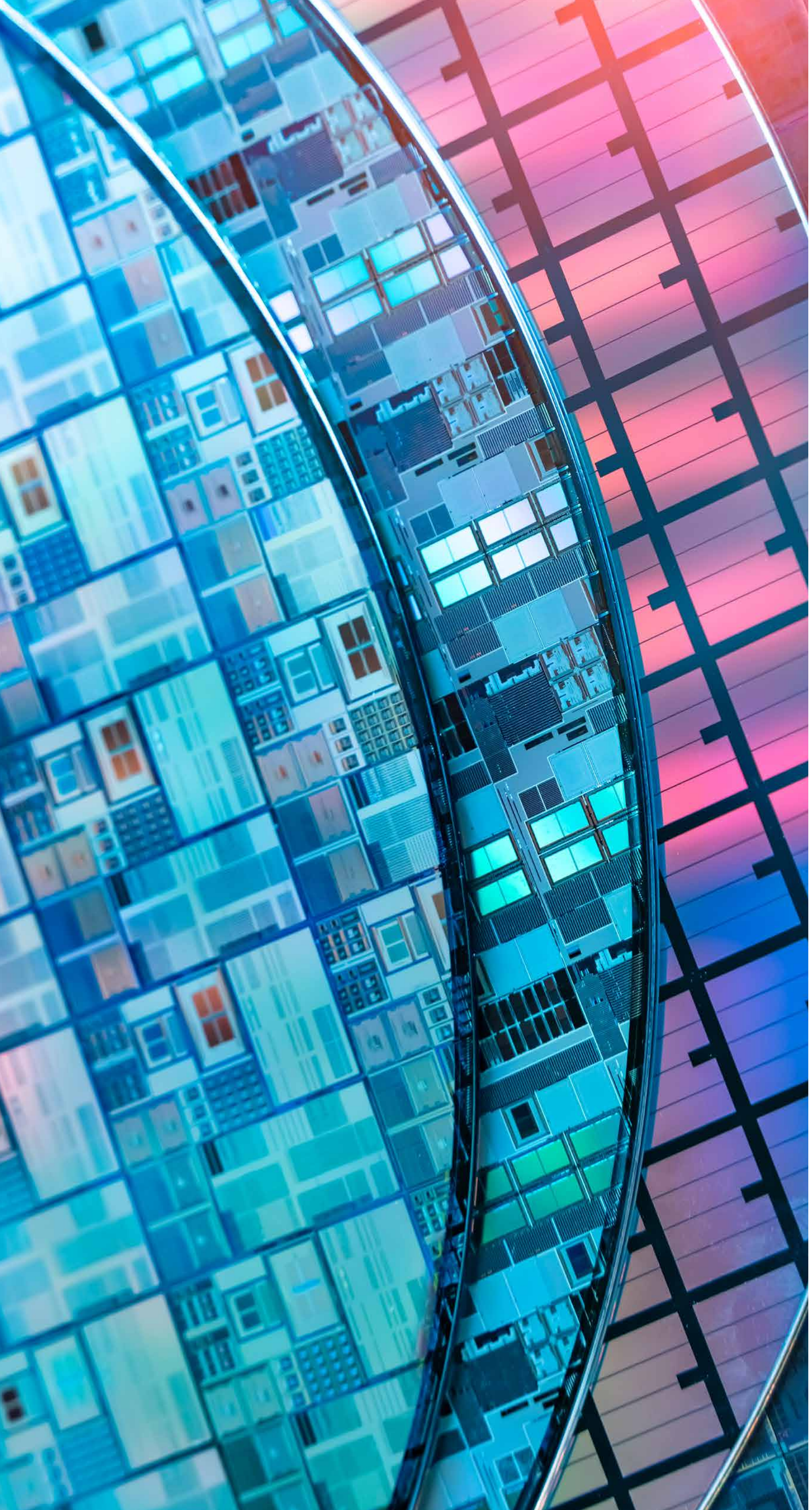


ESD & Latch-up Testing at Eurofins EAG Laboratories

Eurofins EAG Laboratories is an industry leader in Electrostatic Discharge (ESD) and Latch-Up (LU) testing for both classification and characterization. We employ state-of-the-art testing methodologies that are consistent, reproducible, and aligned with the latest industry standards, delivering precise data interpretation and accurate assessment of results.

To further accelerate your time to results, we offer in-house PCB design and rapid fabrication of custom ESD test fixtures. In addition to our comprehensive ESD and Latch-Up testing services, clients have ready access to world-class capabilities across failure analysis, environmental and reliability testing, focused ion beam (FIB) circuit edit, advanced electron microscopy, and automated test equipment (ATE) services. EAG Laboratories has a large capacity of the latest equipment for HBM, CDM, and LU stress testing. Our quality management system conforms to ISO 17025 & 9001:2015-.

Our ESD and Latch-up test offerings include:

- Human Body Model (HBM) - both relay testers and low-parasitic 2-point tester
- Machine Model (MM) for legacy products
- Charged Device Model (CDM) – field charge and direct charge methods
- Latch-up (LU) and High-Power Latch-up (HPLU)
- Transmission Line Pulse (TLP) and Very Fast Transmission Line Pulse (VF TLP)

ESD Testing Services

All ESD testing is performed in strict compliance with JEDEC, MIL-STD, AEC, and ESD Association standards, ensuring consistency, accuracy, and alignment with industry expectations. Eurofins EAG Test Service Levels provide for optimal pricing for the data you need.

Level 1 (Zap Only): HBM and CDM best price – results based solely on final electrical test at your site.

Level 2 (Pre and Post Curve trace): HBM, CDM, LU – DC curve trace comparison done pre and post stress to look for changes in continuity or comparative curve shifts.

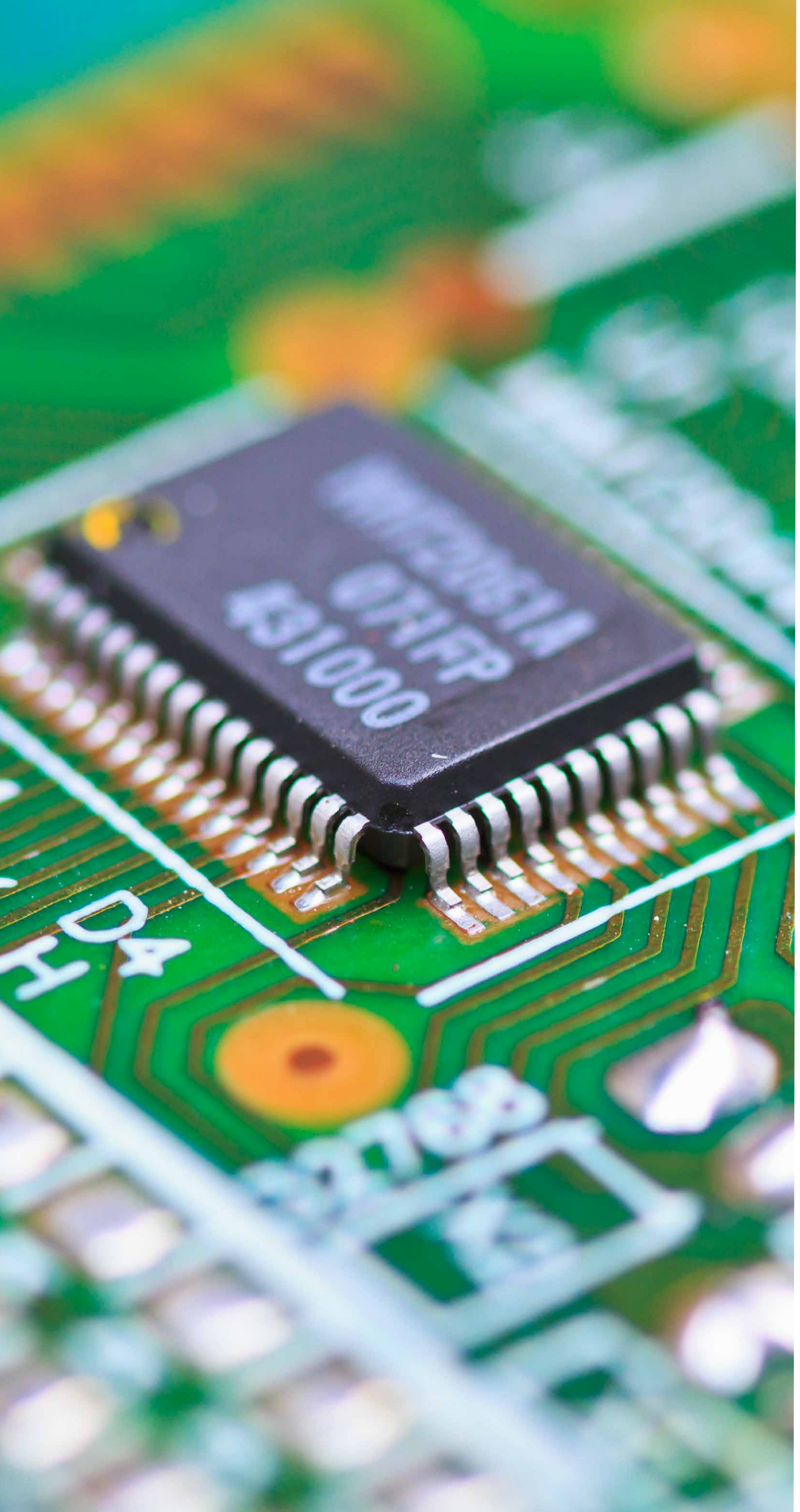
Level 3 (Curve trace after each zap): HBM only – DC curve trace of each pin under test after each stress pulse.

Applicable HBM Specs:

- JEDEC: JS-001-2017 and JESD22-A114 (superseded by JS-001-2024)
- Department of Defense: MIL-STD-883, Method 3015.7
- Automotive Electronics Council: AEC-Q100-002 and AEC-Q101-001 (based on JS-001-2024)
- ESD Association: ESD STM 5.1-1998 (superseded by JS-001-2024)

Applicable CDM Specs:

- JEDEC: JS-002-2018 and JESD22-C101 (superseded by JS-002-2025)
- Automotive Electronics Council: AEC-Q100-011 and AEC-Q101-005 (based on JS-002-2025)
- ESD Association: ESDA STM 5.3.1-1999 (superseded by JS-002-2025)



ESD Testing Services

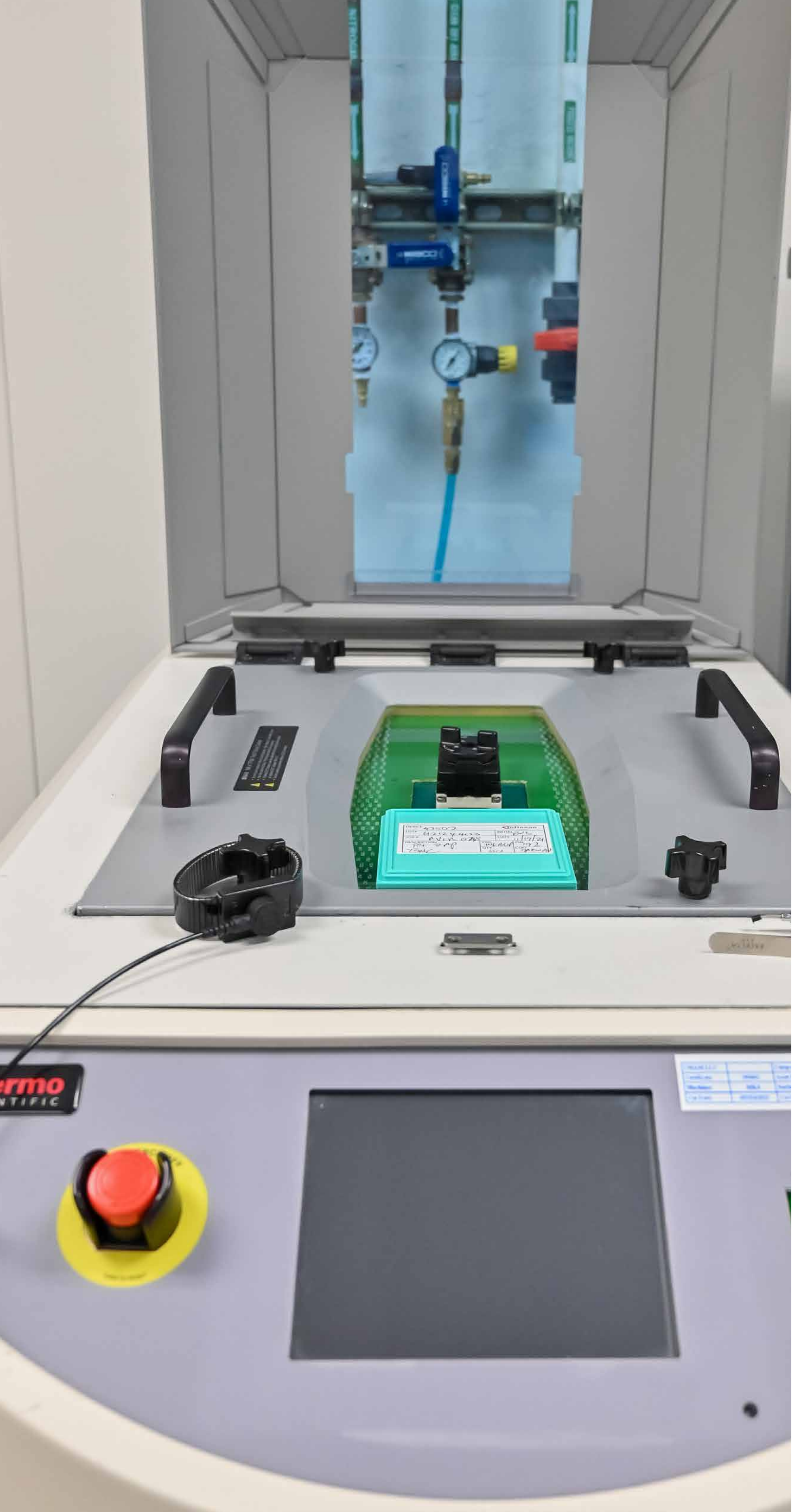
Applicable MM Specs:

- JEDEC: JESD22-A115 (obsoleted by JEDEC, but still available)
- Automotive Electronics Council: AEC-Q100-003 and AEC-Q101-002 (obsoleted by AEC, but still available)
- ESD Association: ESD STM 5.2-1999 (obsoleted by ESDA, but still available)

2-Point Human Body Model Testing (Low Impedance HBM):

Low-impedance 2-point HBM testers enable reliable ESD characterization at both the package and wafer level, making them especially valuable during early prototype evaluation. Beyond standard leakage current measurements before and after stress, these systems also capture real-time voltage and current during the HBM event, providing deeper insight into device behavior under stress.

They additionally help identify and prevent potential “false positives” caused by relay tester parasitics. Altogether, this versatile approach offers a clearer and more comprehensive understanding of true device performance on an individual pin-pair basis.



Latch-Up Testing Services

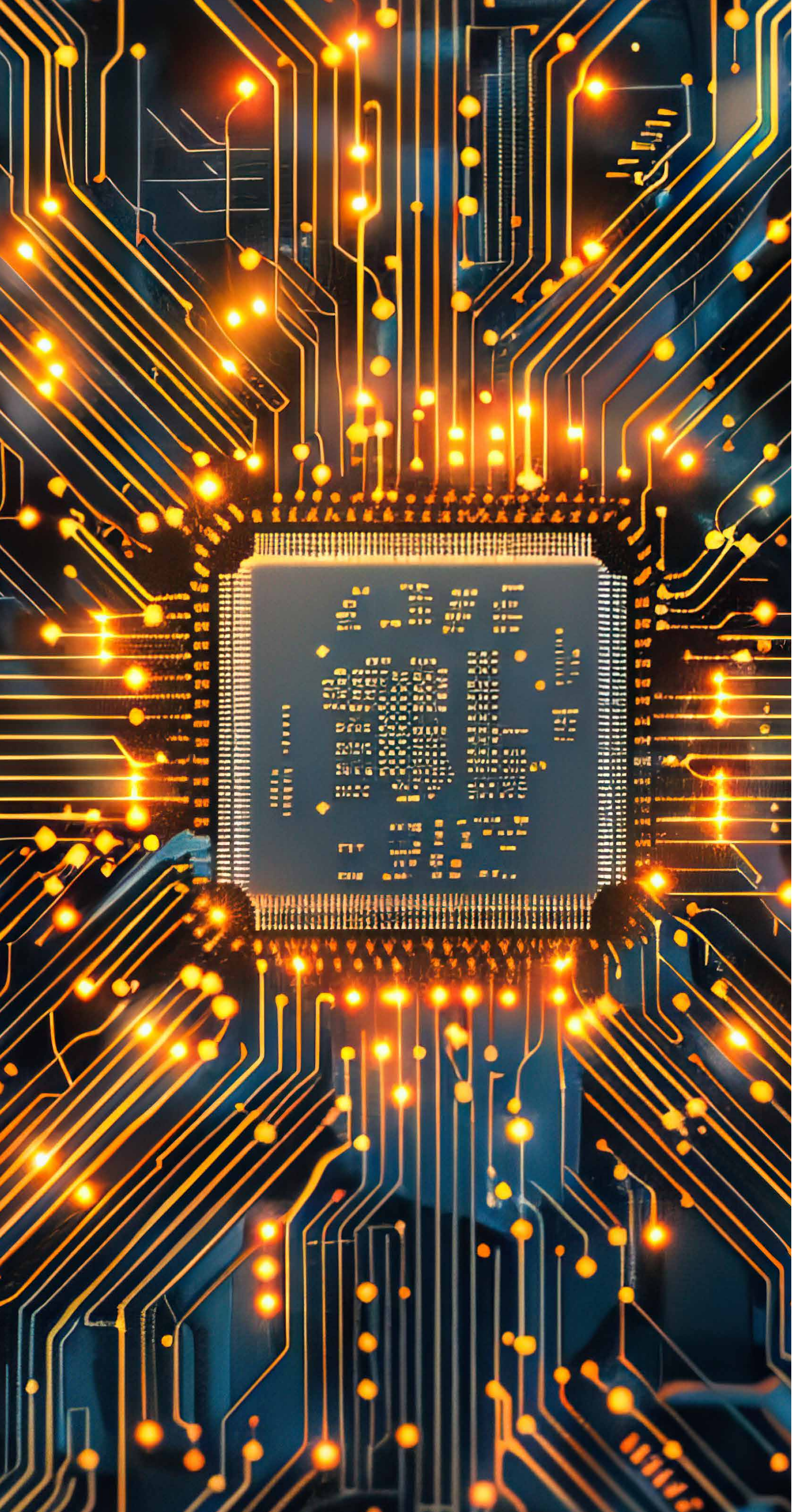
While Latch-Up testing and ESD testing use the same automated testers, their methods differ. ESD testing is an unpowered test, where voltage pulses are applied to device pins in various combinations of grounded and active states on the device under test (DUT). In contrast, Latch-Up testing is conducted with the DUT powered up, with input signals applied, to establish a stable, low-current operating condition.

Latch-Up testing aims to trigger and observe latch-up events caused by parasitic SCR structures in CMOS/Bi-CMOS devices. Results are affected by chip layout and charge handling. Testing is performed in accordance with the latest JEDEC specifications— JESD78F—and can be conducted at customer-specified ambient temperatures ranging from 25°C to 150°C.

Eurofins EAG is one of the few companies that has a long history of running High Power LU (HPLU). This setup allows for any power rail of the unit that draws more than ~8A to be routed externally. Used in conjunction with up to 6 external supplies and temperature stabilizing hardware, this system can perform all LU current injection tests and Supply Overvoltage tests on parts that can draw at currents in excess of 100A.

Applicable LU Specs:

- JESD78 (JEDEC)
- AEC-Q100-004 (Automotive Electronics Council)



Transmission Line Pulse Testing (TLP) & Very Fast Transmission Line (VF TLP) Testing

Transmission Line Pulse (TLP) and Very Fast Transmission Line Pulse (VF TLP) testing are powerful methods for characterizing ESD protection structures in semiconductor devices. Standard TLP pulse widths and rise times are comparable to the HBM waveform. VF TLP pulse and rise times are comparable to the CDM waveform stress.

This type of characterization testing serves two key purposes: Primarily to evaluate ESD inputs protection devices on new process technologies and Intellectual Property (IP), helping to develop accurate simulation parameters and to compare the relative performance of different ESD protection designs. Secondly, this testing is a valuable electrical failure analysis tool, often used in conjunction with conventional, standards-based component ESD testing, to gain deeper insight into device behavior under stress conditions.

TLP testing is performed in accordance with the ESDA TLP test method and is quoted on a case-by-case basis, depending on the scope of work, required engineering time, and customer-specific reporting needs.

Applicable TLP Specs:

- TLP – ANSI/ESD STM5.5.1-2022
- VF TLP – ANSI/ESD SP5.5.2-2007

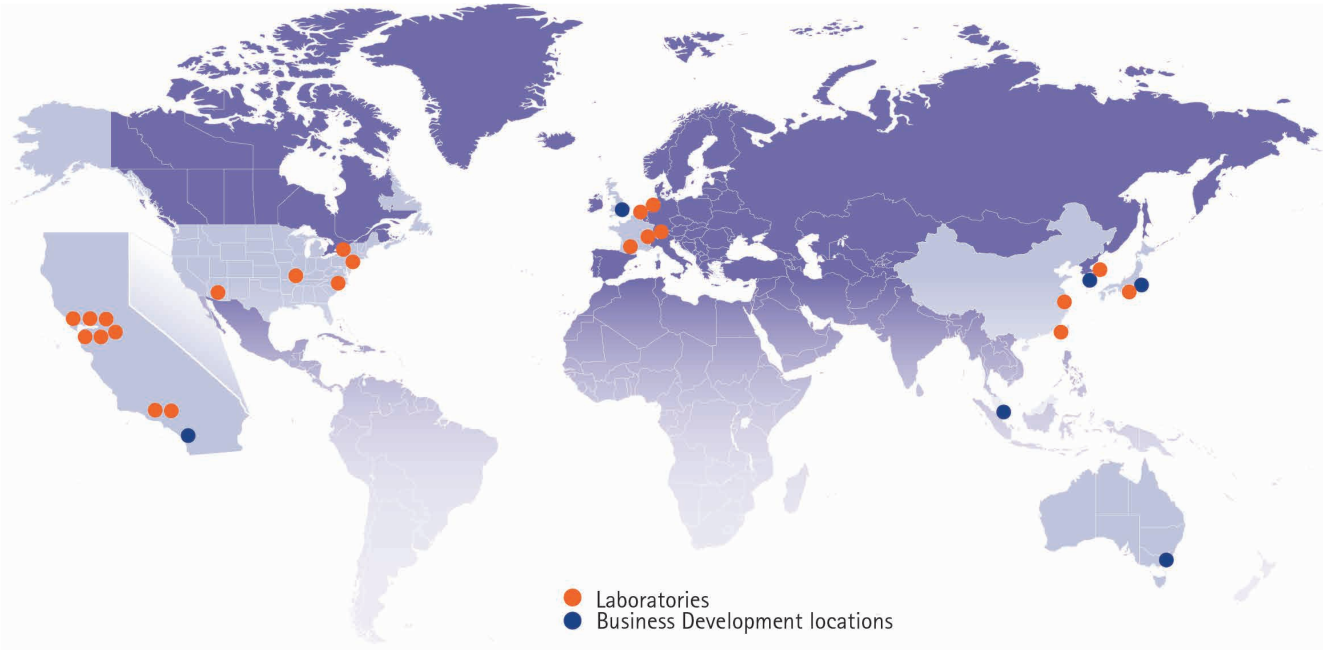
Why Choose Eurofins EAG Laboratories?

Eurofins EAG Laboratories offers a comprehensive suite of engineering services to support all phases of semiconductor product development. Our capabilities span ATE test development, pilot and production testing, burn-in and reliability qualification, ESD and Latch-Up testing, debug and FIB circuit edit, advanced failure analysis, and state-of-the-art microscopy (SEM, TEM, FIB/SEM). We also provide in-house PCB design and hardware development to accelerate testing and analysis workflows.

With deep expertise in ESD and Latch-Up testing for advanced semiconductor technologies, we deliver comprehensive HBM, MM, CDM, Latch-Up, and TLP services, along with expert data interpretation and detailed results analysis. Our customized test solutions help clients fill equipment and expertise gaps, manage risk, and accelerate time to market. In addition, our industry-leading failure analysis capabilities enable rapid root cause identification and resolution, ensuring product reliability and performance.

Whether you're developing next-generation ICs or addressing reliability concerns, Eurofins EAG is your trusted partner for high quality testing, analysis, and engineering insight.

Scan here to learn more about our services and capabilities.



About Eurofins EAG Laboratories

When it comes to understanding the physical structure, performance, chemical properties and composition of materials, no other scientific services company offers the breadth of experience, diversity of analytical techniques or technical ingenuity of Eurofins EAG Laboratories. We don't just perform testing, we drive commercial success—through thoughtfully designed investigations, technically superior analyses, and expert interpretation of data.

We deliver multi-disciplinary, problem-solving expertise to help our customers accelerate innovation, ensure quality and safety, and protect intellectual property. Whether you are seeking to reduce time-to-market, solve manufacturing problems or ensure regulatory compliance, turn to Eurofins EAG. We know how to bring the power of science to every phase of your product lifecycle.

- 20+ facilities located in the US, Europe, and Asia
- 2,500+ instruments
- 1,000+ highly-educated employees
- Serving more than 5,000 clients worldwide
- Revenue sourced from more than 50 countries

Complete Lifecycle of Services

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